



# Specification, Measurement, and Control of Electrical Switching Transients

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Prepared for Marshall Space Flight Center  
under Contract H-29919D  
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the Space Environments and Effects Program  
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## EXECUTIVE SUMMARY

This investigation into the nature and control of electrical power bus load-induced switching transients was performed under contract to the National Aeronautics and Space Administration (NASA) through its Space Environments and Effects (SEE) Program. The contract number was H29919D.

The investigation developed two pieces of test equipment which provide accurate and repeatable measurement and generation of switching transients. Combined with the guidelines for specifying limits contained herein, the result of the investigation is a complete solution to the problem of controlling the generation of and response to electrical power bus switching transients.

## ACRONYM LIST

ARP	Aerospace Recommended Practice
ccw	counter-clockwise
CE07	MIL-STD-461B/C conducted emission limit on switching transients
CMRN	common mode rejection network (equivalent to DMSN)
CS06	MIL-STD-461 through Rev. C conducted susceptibility test, spikes on EUT input power leads
CS115	MIL-STD-461D/E conducted susceptibility requirement, trapezoidal pulse coupled to cables
CS116	MIL-STD-461D/E conducted susceptibility requirement, damped sinusoid coupled to cables
DIP	dual in-line package
DMSN	differential mode selection network (equivalent to CMRN)
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EMP	electromagnetic pulse
EUT	equipment-under-test
FET	field effect transistor
I/O	input/output
LeRC	Lewis Research Center (NASA) Cleveland, Ohio
LISN	line impedance stabilization (or simulation) network
MSFC	Marshall Space Flight Center (NASA) Huntsville, Alabama
NASA	National Aeronautics and Space Administration
NC/NO	in reference to relays: normally closed/normally open
NSTS	National Space Transportation System - (Space Shuttle)
PCB	printed circuit board
PDS	power distribution system (power bus)
pps	pulses per second
PSU	power switching unit (emission switch sub-unit that switches power from LISN to EUT)
RAU	Remote Acquisition Unit (Spacelab equipment and communication/control system interface)
RTCA	Radio Technical Commission for Aeronautics
SAE	Society of Automotive Engineers
SEE	Space Environments and Effects
STS	switching transient simulator (name given to spike generator described in Appendix E)
TT01	NASA requirement/test method for measuring load induced power bus switching transients

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# Specification, Measurement, and Control of Electrical Switching Transients

## 1. INTRODUCTION

This report describes the phenomena of electrical power bus transients induced by the switching of loads both on and off the bus, and the control thereof. Such transients will hereinafter be termed (load-induced) switching transients.

This report has three main sections and five appendices. It is organized as follows.

Section 1: Historical background and physical description of load-induced switching transients on electrical power buses

Section 2: Detailed numerical description of switching transients

Section 3: Issues related to levying limits on switching transient emission or susceptibility

There are five appendices:

Appendix A is a test requirement/test procedure for measuring the emission of switching transients modeled after the format of SAE ARP 1972, "Recommended EMC Test Procedures."

Appendix B is a test requirement/test procedure for measuring switching transient inrush current modeled after the format of SAE ARP 1972, "Recommended EMC Test Procedures."

Appendix C is a test requirement/test procedure for measuring susceptibility to switching transients modeled after the format of SAE ARP 1972, "Recommended EMC Test Procedures."

Appendix D is a manual for operation of the Precision Phase-Controlled Power Switch used for producing repeatable worst-case switching transient emissions. It includes detailed test procedures, theory of operation, parts description, and a schematic.

Appendix E is a manual for operation of the Switching Transient Generator used for producing simulated switching transients for the purpose of evaluating susceptibility. It includes detailed test procedures, theory of operation, parts description, and a schematic.

### 1.0.1 RATIONALE FOR SWITCHING TRANSIENT CONTROL

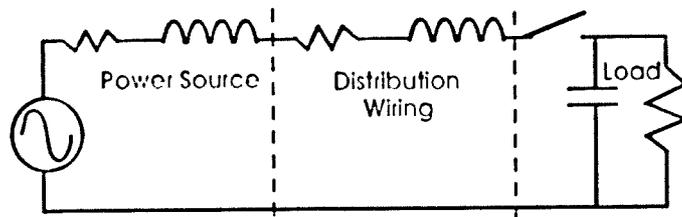
There have been several instances of susceptibility to switching transients. The Space Shuttle Spacelab Remote Acquisition Unit (RAU - a standard interface between Spacelab payloads and the Shuttle communications system) will shut down if the input 28 Vdc bus drops below 22 Volts for more than 80  $\mu$ s. Although a MIL-STD-461 derivative CS06 requirement was levied on the RAU, it failed to find this susceptibility. A heavy payload on one aircraft sags the 28 Volt bus below 20 Volts for milliseconds. Vacuum cleaners which plugged into Spacelab 400 Hz bus sagged the line potential enough that computers also powered by 400 Hz crashed. Dc-dc converters have an operating voltage range. For instance, a typical 28 Vdc-to-5 Vdc converter operates within tolerance when input potential is between 17 - 40 Vdc. A hold-up capacitor can be used to extend the time this range is presented to the converter when the line potential sags or surges outside this range. The designer must know the range of normal transients in order to choose the correct value of hold-up.

### 1.0.2 PHYSICS OF LOAD INDUCED SWITCHING TRANSIENTS

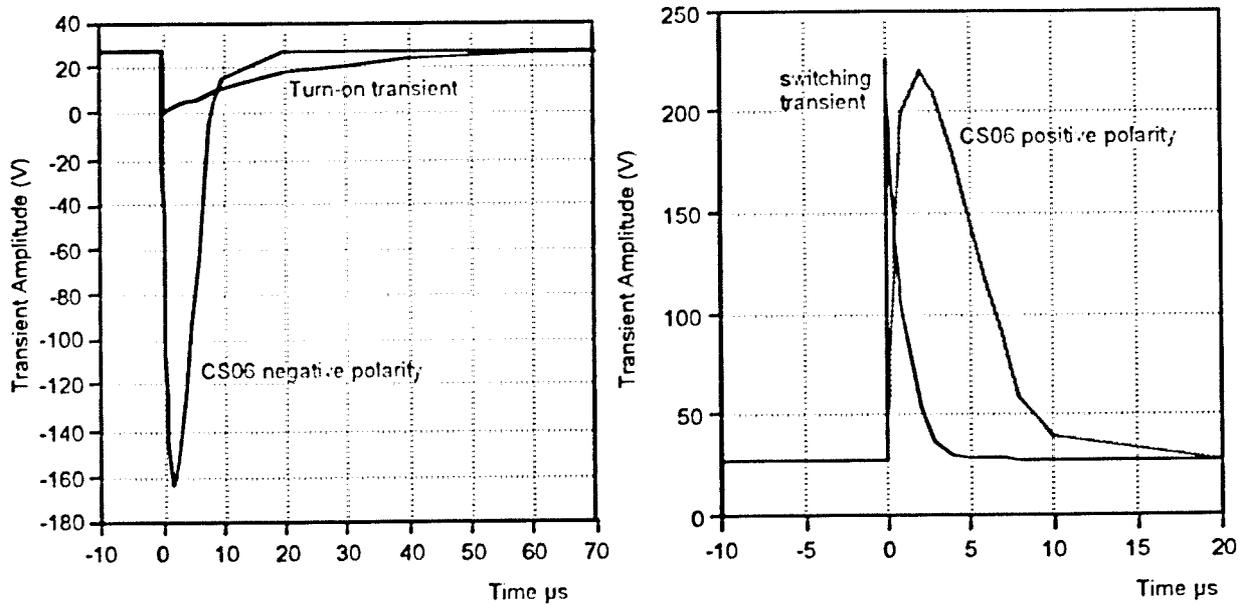
Figure 1 portrays the elements of a power distribution system. There is a power source, distribution wiring, and a load. The power source may be simplified to an ideal voltage source in series with a resistive and/or inductive impedance. The distribution wiring contributes both

## Specification, Measurement, and Control of Electrical Switching Transients

resistance and inductance. The load, at turn-on or turn-off, attempts to generate a rapid change of current through the power source and wiring impedance. Load capacitance is a short circuit to ground at the instant it is connected to the bus. The distribution wiring inductance impedes this current demand by generating a potential of such polarity as to oppose the flow of new current. The resultant waveforms are depicted in Figures 2a and b. This simple model ignores any capacitive effects, other than the load. Source parallel capacitance (especially in a dc supply) contributes to source stiffness, which may be easily modeled in the transient case by using a smaller series source impedance. Line-to-line or line-to-ground wiring capacitance is easily accounted for by modeling the distribution wiring as an inductance bypassed by a resistor. That is to say, a lumped element model of a transmission line, otherwise known as a line impedance stabilization network, (LISN). Figure 3 shows a model for both calculating and measuring switching transients. In Figure 3, the LISN models the distribution wiring impedance.



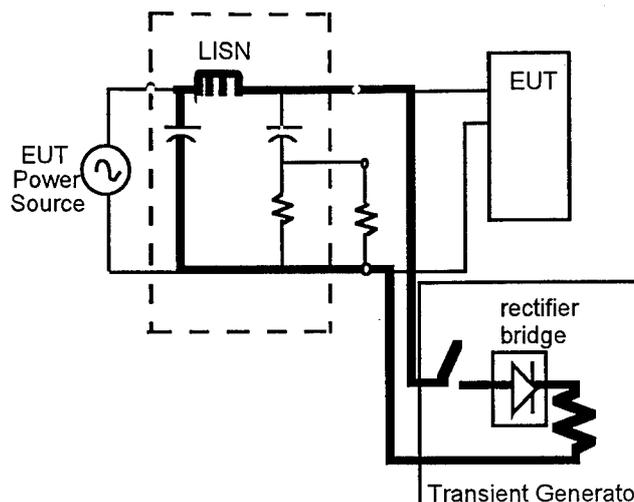
**Figure 1:** Model of electrical power distribution system



*a. turn-on switching transient and CS06 negative polarity*

*b. turn-off transient vs. CS06 positive polarity*

**Figure 2:** Turn-on and turn-off transients envelopes: 28 Vdc bus, 50  $\mu$ H, 50  $\Omega$  LISN, 7  $\Omega$  //100  $\mu$ F load vs. CS06 10  $\mu$ s transient waveform



**Figure 3:** *Spike generator model: Heavy lines show flow of high current to spike generating load.*

### 1.1 PURPOSE

The purpose of this report is to provide a complete path to providing specification control of the switching transient phenomenon. Such control requires:

- complete physical description of the phenomenon of switching transients. This includes waveform amplitude vs. time envelopes, as well as source impedance. Such power quality standards as MIL-STD-704 often depict envelopes symmetrical about the zero amplitude axis. As developed herein, it will be apparent that no such symmetry exists.
- accurate, repeatable measurement of load-induced switching transients. Such requirements/test techniques have been variously labeled CE07 (MIL-STD-461B/C) or TT01 (National Space Transportation System - Space Shuttle). Both of these precursor requirements suffered significant imperfections. CE07 was a requirement without a test technique. TT01 provides a test technique, but allows enough latitude in LISN (line impedance simulation network) design and switch implementation that interpretation of test data is often problematical.
- accurate representation of load-induced switching transients to evaluate and control the susceptibility of power bus loads. A previous attempt at such control was MIL-STD-461A/B/C requirement and test method CS06. Again, as shall be developed herein, CS06 was an imperfect model of switching transients.

This report fully characterizes switching transients, describes a well-controlled test to measure load-induced switching transients, and also describes a well-controlled test to generate such transients for susceptibility testing. These requirements and test methods are fully tailorable. That is, based on expected bus performance, the requirement and test technique can be modified to provide appropriate waveforms. This report fully describes the test equipment necessary to fulfill these requirements. This equipment was developed to support this investigation.

### 1.2 BACKGROUND

In 1994, the author presented a paper at the IEEE EMC Symposium entitled "Specifying Control of Immunity to Power-Line Switching Transients." In that paper, the author developed a feasibility-study breadboard circuit that would generate simulated switching transients. In this

report, that circuit has been upgraded to the quality of bench top test equipment (essentially, a replacement for the Solar Model 8282-1 CS06 spike generator when switching transients are of sole interest.) In addition, a separate switch has been developed, similar to the first, that switches the EUT (equipment-under-test) on/off in a repeatable manner for accurate transient emission characterization. This is also bench top quality test equipment. Material from the 1994 paper is used throughout this report.

Several years ago the author developed detailed CE07 test procedures for an update of SAE ARP 1972, Recommended EMC Test Procedures. The author specified, but did not provide detailed design of an emission switch (for cycling the EUT on/off). NASA's Lewis Research Center (LeRC) volunteered to design such a switch. The author evaluated a working model provided by LeRC. The LeRC model provided the necessary functions and this investigation further simplified the design.

### 1.3 SCOPE/DISCLAIMER

This report addresses the control of switching transients. Externally induced transients such as lightning, EMP (electromagnetic pulse) or other field-to-wire coupling are not discussed. Whereas in this report the susceptibility spike generator will be shown to be superior to the CS06 spike source (such as the Solar Model 8282-1), this is only true with respect to switching transients. If lightning or other low impedance phenomena are of concern, then the 8282-1 is the right approach. Likewise, if field-to-wire coupling is of interest, then 50  $\Omega$  sources such as MIL-STD-461E CS115/CS116 or RTCA/DO-160 Section 17 are the correct approach. All statements made herein regarding the superiority of the developed equipment must be understood to pertain solely to the simulation and control of load-induced switching transients.

## 2. FULL DESCRIPTION OF THE SWITCHING TRANSIENT PHENOMENON

The transient generating mechanism is the switching on/off of a heavy load while the EUT is in steady-state operation. The LISN is the common impedance to the EUT and the switched load. Qualitative analysis of the on/off transients is now presented.

### 2.1 THE TURN-ON, OR NEGATIVE GOING TRANSIENT

The initial condition is that the load switch is open and no current is flowing in the switched load. The EUT is on and in steady-state operation. Upon switch closure current attempts to flow through the load. The LISN inductance opposes the change in the current by dropping the source voltage across itself. The LISN output voltage momentarily dips to near zero, and then gradually increases as the inductor relaxes. The transient time constant is a function of the LISN inductance and the RC time constant of the load, with oscillations due to inductor-capacitor energy transfer. The source impedance of the transient is the impedance of the switched load. In this analysis, the supply voltage is 28 Vdc, and the load bank is 7  $\Omega$  paralleled by 100  $\mu$ F, drawing 4 Amps after the capacitor charges. The turn-on transient for these conditions is shown in Figure 2a.

### 2.2 THE TURN-OFF, OR POSITIVE GOING TRANSIENT

The initial condition is that the load has been on long enough to achieve steady-state 4 Amp dc current flow. The switch is abruptly opened. If the switch risetime is fast enough to be in the 50

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$\Omega$  frequency domain of the LISN, and the LISN provides a reliable 50  $\Omega$  at all frequencies of interest above the knee frequency, the calculation is once again straightforward. The LISN 50  $\mu$ H inductor tries to maintain the 4 Amp current flow through itself. It does this by raising the voltage at the output of the LISN relative to the input. (Incidentally, this phenomenon answers the oft-raised question about spike tests: "Does the specified spike amplitude include the line voltage, or is it superimposed on the line voltage?" The line inductance superimposes the spike voltage on the power line voltage, or it would not have the desired effect of maintaining the current through the inductance). If the inductor were the only element to consider, the spike induced by turning off the load would be infinite in amplitude. However, reality imposes line-to-line and other stray capacity which would tend to snub the spike. A benefit of the 50  $\Omega$  LISN is that the 50  $\Omega$  dummy load provides a stronger snubbing effect than any stray capacity, yielding repeatable, predictable spikes. Per our assumption, we are in the 50  $\Omega$  frequency domain of the LISN; then the spike voltage is just the switched current multiplied by 50  $\Omega$ . In our case, we should see a 200 Volt spike (50  $\Omega$  x 4 Amps). The time constant is independent of the load impedance, it has been switched out of the circuit. The time constant is the ratio of the 50  $\mu$ H inductor and the 50  $\Omega$  dummy load, or one microsecond. The source impedance is 50  $\Omega$ . The qualitatively predicted waveform is shown in Figure 2b.

It is interesting to calculate the spike amplitude, duration and source impedance as a function of a varying dummy load impedance. If the dummy load were, for instance, 5  $\Omega$ , then spike amplitude (for the same switched 4 Amps) would be 20 Volts, time duration would be 10  $\mu$ s, and the source impedance would be 5  $\Omega$ . A figure of merit related to spike energy may be calculated as follows. Take the product of spike amplitude by spike short circuit current by spike time constant. This is Volts times Amps times time duration. In the above 50  $\Omega$  and 5  $\Omega$  cases, we get an unvarying 0.5 millijoule. This is reassuring: the amount of *energy* stored in an inductor is

$$\frac{1}{2} L I^2,$$

and only the rate of discharge should be affected by the parallel resistance.

### 2.3 SUMMARY OF SWITCHING TRANSIENT CHARACTERIZATION AND COMPARISON TO CS06 SPIKE GENERATOR CHARACTERISTICS

Before proceeding to test data to verify the foregoing analysis, it would be valuable to summarize the predictions made. Figure 1 serves as a graphical summary and comparison of our predictions to the common spike immunity requirement, MIL-STD-461 CS06. A negative-going transient due to a load coming on-line will have a maximum amplitude excursion near zero, the source impedance of the switched load, and a time constant related to the LISN inductance and load capacitance and resistance. A positive going transient will have an amplitude of the switched current multiplied by the LISN bypass resistance, a source impedance equal to the bypass resistance, and a time constant given by the ratio of LISN inductance and bypass resistance. The MIL-STD-461 CS06 10  $\mu$ s spike has fixed amplitude, time duration, and 1  $\Omega$  or less source impedance, regardless of polarity.<sup>1</sup>

---

<sup>1</sup>The Solar 8282-1 CS06 spike generator is specified to have the following output impedances:

10  $\mu$ s - < 1  $\Omega$ ; 5  $\mu$ s - < 2  $\Omega$ ; 0.15  $\mu$ s - < 5  $\Omega$ .

### 3. SPECIFYING CONTROL OF THE SWITCHING TRANSIENT PHENOMENON

It can be seen from the foregoing discussion that switching transient magnitude (amplitude, time duration) can be estimated from a knowledge of bus characteristics including nominal bus potential and bus impedance. The following facts are immediately discernable.

#### 3.1 TURN-ON TRANSIENTS

These transients depart nearly instantaneously from nominal bus potential towards zero potential, then gradually return to nominal following a (typically) underdamped exponential decay. The generic shape is that of the negative going long duration transient shown in Figure 2a. The excursion never dips below zero. The time to return to nominal depends on the reactive elements of the switched load (mainly line-to-line capacitance) and the reactive and resistive impedance of the power bus. Once a LISN model has been developed, as well as a typical, or reasonable worst-case model of a switched load, the turn-on transient envelope can be determined using analytical techniques (SPICE) or the test equipment described herein.

The subject of safety margins must be addressed (a detailed numerical example is provided in Appendix E). It is common to calculate a predicted emission and multiply this by a safety factor to determine a susceptibility limit. While this approach has some value, it must be carefully applied in the case of the turn-on switching transient. Because the transient physically cannot dip below zero, there is no point in providing a safety margin via amplitude multiplication. In any case, the equipment protected by levying CE07/TT01 control is generally built to operate in some amplitude band centered on nominal bus potential. If the bus potential exceeds these bounds, it is not the magnitude of the excursion but rather the duration which is critical. Therefore, if a safety margin is desired, it should be applied to the duration of the transient, rather than the amplitude.

If the bus is ac, then the magnitude of the transient is strongly a function of the power waveform amplitude at the moment of turn-on. Therefore it is of crucial importance that the test technique be capable of selecting and repeating turn-on at any portion of the waveform.

##### 3.1.1 MEASUREMENT OF INRUSH CURRENT

Related to the concern over switching transient amplitude vs. time control is the need to (often) control inrush current. This can be important on current limited buses, but also to ensure that a fuse-protected load will not fuse open upon turn-on. In such cases, it is important to accurately measure the peak current that the EUT can possibly draw. This is accomplished by replacing a LISN with a low impedance (stiff) power source. The stiffness is ascertained by monitoring potential sag during EUT turn-on. The sag must be bounded. This is fully developed in the appropriate appendix (B). With regards to an ac bus, the magnitude of the inrush current is strongly a function of the power waveform amplitude at the moment of turn-on. Therefore it is again of crucial importance that the test technique be capable of selecting and repeating turn-on at any portion of the waveform.

#### 3.2 TURN-OFF TRANSIENTS

These transients depart nearly instantaneously from nominal bus potential in a positive fashion (that is, increasing potential). Fundamentally, the amplitude of the transient is the inductance of the bus multiplied by the rate of change of current. Given two reasonable assumptions, this

calculation is greatly simplified. A LISN bus model bypasses the bus inductance with a resistive high frequency asymptote (typically 50  $\Omega$  or 100  $\Omega$ ). If the load is switched fast enough that the spectrum falls within the resistive asymptote range of the LISN impedance Bode plot, then the resulting switching transient amplitude is simply the switched current amplitude multiplied by the LISN high frequency resistance (Figure 2b). Further, the duration of the transient is independent of the switched load. Duration is solely a function of the LISN L/R time constant. It is for this reason that imposition of an emission limit for turn-off transients is problematical. Given a particular LISN model and a steady-state current draw, the only way to design to meet a turn-off transient requirement is to control the rate of change current draw. This is only possible if the turn-off command originates in, and is executed within the EUT. As is the case for turn-on transients, if the bus is ac, then the magnitude of the transient is strongly a function of the power waveform amplitude at the moment of turn-on. Therefore it is of crucial importance that the test technique be capable of selecting and repeating turn-on at any portion of the waveform.

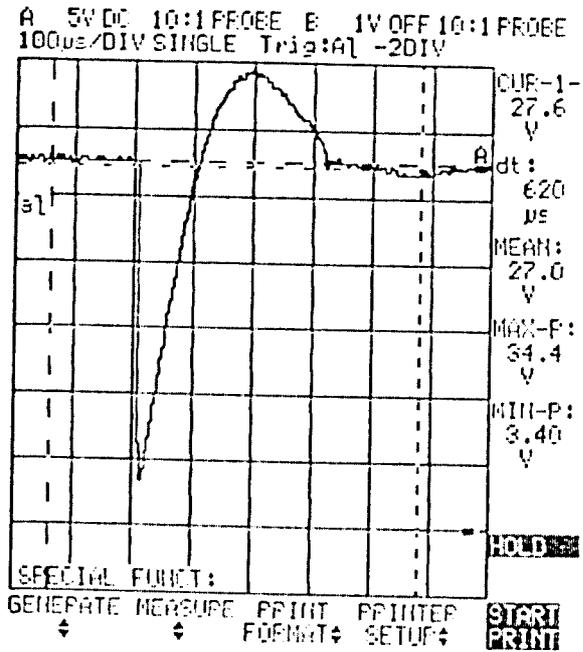
### 3.3 NOTE CONCERNING TRANSIENT LIMITS AS A FUNCTION OF BUS POTENTIAL

The following conclusion is quoted from the 1994 paper on the subject of switching transients.

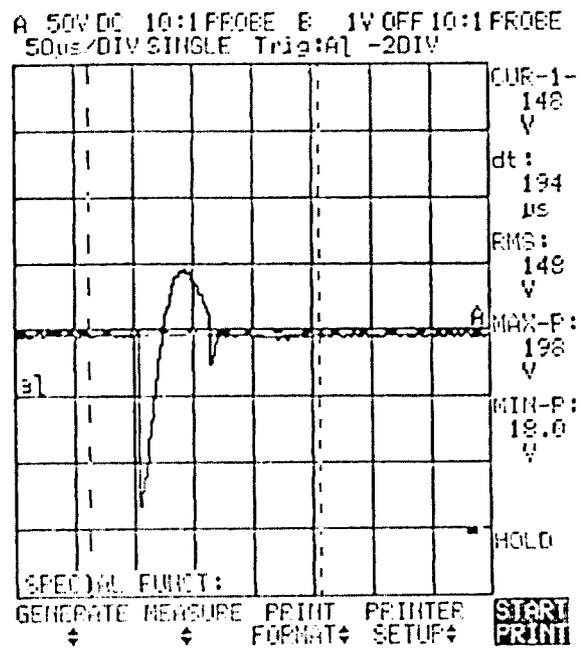
"The proposed test method and specification yield a spike immunity requirement tailored specifically for switching transients. Equipment transient emissions may be directly compared to the immunity limit to assess margins; in this way reasonable emissions/ susceptibility limits may be generated. Loads on a low voltage bus will induce transient waveforms of higher positive magnitudes, and longer duration negative spikes, than similar power loads on a higher voltage bus. Therefore, switching transient emission and immunity limits may be specified more benignly for higher voltage buses."

Note that this conclusion stands in stark contrast to the usual CS06 tailoring which often ties spike potential to bus potential. In the test data shown below, equal power loads were switched from 28 Vdc and 120 Vdc (actually 150 Vdc, but loads were calculated for 28 and 120 Vdc). It is readily apparent that the 28 Vdc switched load (oscillographs 1 and 3) generates a longer turn-on transient and a much higher amplitude turn-off transient than the same power load on 120 Vdc (oscillographs 2 and 4). 28 Vdc load was picked as convenient (10  $\Omega$ //100  $\mu$ F). The 120 Vdc load resistance is 160  $\Omega$ , which draws equal power from 120 Vdc as 10  $\Omega$  does from 28 Vdc. The 120 Vdc capacitor was picked to yield the same hold-up time constant as does the 100  $\mu$ F//10  $\Omega$  on 28 Vdc. Note that this is very conservative: given that turn-on transients are shorter on the bus of higher potential, a shorter hold-up time and consequently smaller hold-up cap could have been selected. In turn, the 120 Vdc turn-on transient would have been even shorter than shown in oscillograph 2.

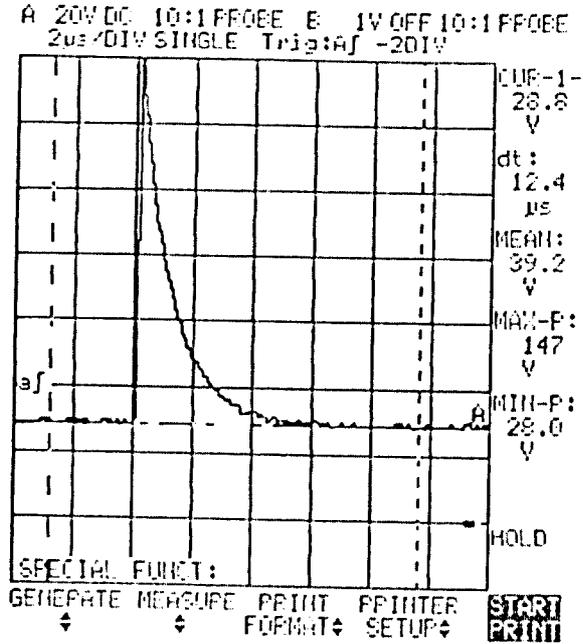
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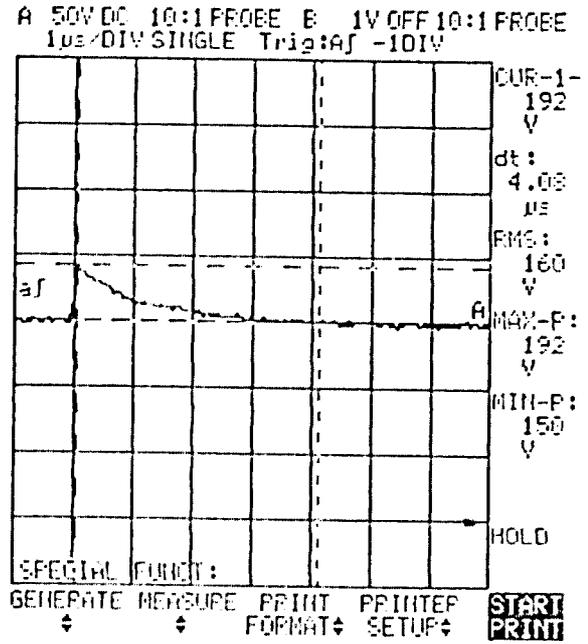
**Oscilloscope 1: 28 Vdc turn-on transient**



**Oscilloscope 2: 120 Vdc turn-on transient**



**Oscilloscope 3: 28 Vdc turn-off transient**



**Oscilloscope 4: 120 Vdc turn-off transient**

## APPENDIX A: CONTROL OF LOAD-INDUCED SWITCHING TRANSIENT EMISSION

### A1 BACKGROUND AND PHILOSOPHY

This time domain test method measures the load induced effect on power bus voltage caused by cycling the EUT on and off, as well as through any and all of its various modes of operation which might reasonably be expected to affect line voltage significantly, that is, in a manner approaching limits set forth in the governing power quality specification.

Several issues are potentially of interest when cycling loads on/off a power bus. This method addresses voltage transients on the bus due to transmission line characteristics of power bus wiring. Another issue is inrush current, which is an important consideration on some types of loads and also when power source is current limited, such as on some space platforms. This issue is addressed under a separate test method.

### A2 RECOMMENDATION

A LISN based test method is desirable since it is the reaction of power bus wiring to rapid changes in current flow that is of interest. The voltage waveform of interest is differential or line-to-line. Therefore, measurement at each LISN EMI port quantifies only one half the waveform. If there is a significant common mode spike measured at each LISN (due to the charging of line-to-ground capacitors), it may be necessary to measure only the differential mode component, using a common mode rejection network (CMRN).

### A3 JUSTIFICATION

- 1) Each LISN EMI port is loaded by  $50 \Omega$  in order that power source impedance responsible for spike be  $100 \Omega$ .
- 2) Transient limit is stated as a ratio to nominal line voltage. Because the EMI port high pass filters nominal line voltage, transient voltage as measured at EMI port is directly comparable to limit. Limit setting activity must take into account that test method measures only one half total transient amplitude.
- 3) If energizing switch is external to EUT, then it must be placed between EUT and LISN. It has been argued that the switch is not under designer's control, and thus he is not responsible for switch produced transients. Switch can only cause two problems. It can bounce on turn-on or turn off too fast or arc on turn-off. Turn-on bounce may be eliminated through use of a mercury switch (does arc), possibly a knife-edge switch, or solid-state switch. The solid state switch described in Appendix B eliminates all concerns regarding switch-contributed noise. Turn-off transient is solely a function of three parameters: EUT load current magnitude just prior to instant of turn-off, how fast current is interrupted, and LISN characteristics. Unless switch is resident in EUT, designer has no control and cannot be held responsible for magnitude of turn-off transient. Data is for information only.

#### A3.1 REQUIREMENT

In order to set a limit, estimate the typical or reasonable worst case load resistance/capacitance that might be switched on or off the bus. Estimate bus impedance (pick a

## Appendix A: Control of Load-Induced Switching Transient Emission

LISN). Use analytical or experimental techniques (utilizing test equipment described in Appendices D/E) to determine transient envelopes. Considering the nature of a power bus, it is difficult to understand how transient can cause line voltage to cross zero from whatever polarity the nominal line voltage happened to be at instant of turn-on. There does not seem to be a justification for a dc limit below zero.

### A3.2 APPLICABILITY

Requirement is applicable for measurement of all turn-on and mode-switching transients. It is only applicable to turn-off transients if switch is part of EUT.

### A3.3 APPARATUS

- a. LISN
- b. Oscilloscope (10 MHz single event bandwidth)
- c. Switch (to energize/de-energize EUT; for ac EUT, switch must turn-on/off at peak of ac waveform)
- d. Recording Device (to store oscilloscope trace/oscillograph)
- e. Triggering Device (trigger analog scope from switched EUT power)

### A3.4 TEST PROCEDURE

- a. Typical test setup is shown in Figures A3-1 and A3-2. Either oscilloscope can be configured for a differential measurement, or a special purpose device (known as a differential mode selection network - DMSN or common mode rejection network - CMRN) can be used which allows a single-ended oscilloscope measurement.
- b. Oscilloscope has at least a 10 MHz single-event bandwidth.
- c. Cycle EUT power on/off and exercise all appropriate internal EUT mode switches. Record voltage transients. Compare against transient specification. If outages occur, see "Additional Instructions" for troubleshooting ideas.

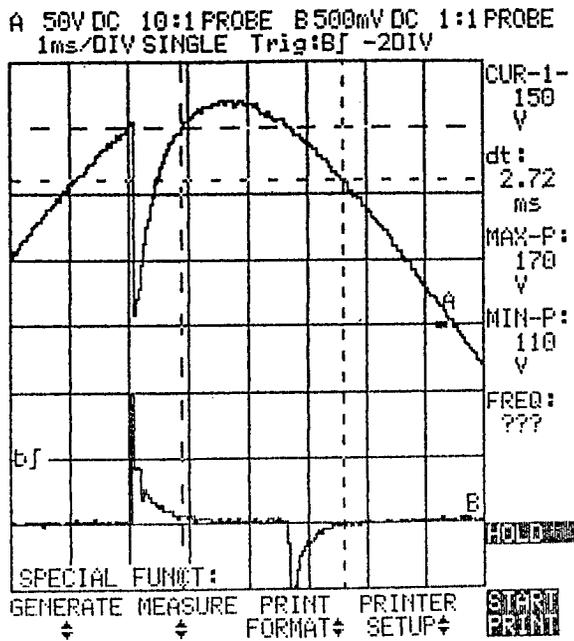
### A3.5 SPECIAL TOPICS

Following issues are unique to time domain transient tests and are important to their successful measurement.

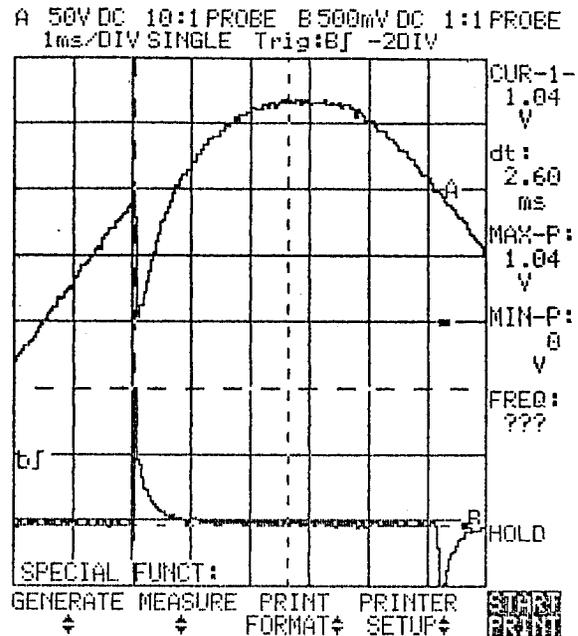
#### A3.5.1 TIMING OF TURN-ON/OFF EVENT

On ac powered EUTs, it is important to cycle EUT's power near the peak (within 10%) of voltage waveform in order to maximize inrush current  $di/dt$ . A special switch, analogous to a zero-crossing switch may be built for this function. The only difference in operation is a 90° phase shift in switching point. Absent such a switch, a lot of data will be taken on a hit or miss basis. A solid state switch is necessary for ac power, since timing must be accurate within  $\pm 1$  ms of a 60 Hz and  $\pm 150$   $\mu$ s of a 400 Hz peak. This switch was developed for this study and is described as to construction and use in the test equipment section. This switch is also used for dc buses, since it does not arc or bounce. Test data below shows how to make accurate ac and dc transient measurements.

## Appendix A: Control of Load-Induced Switching Transient Emission

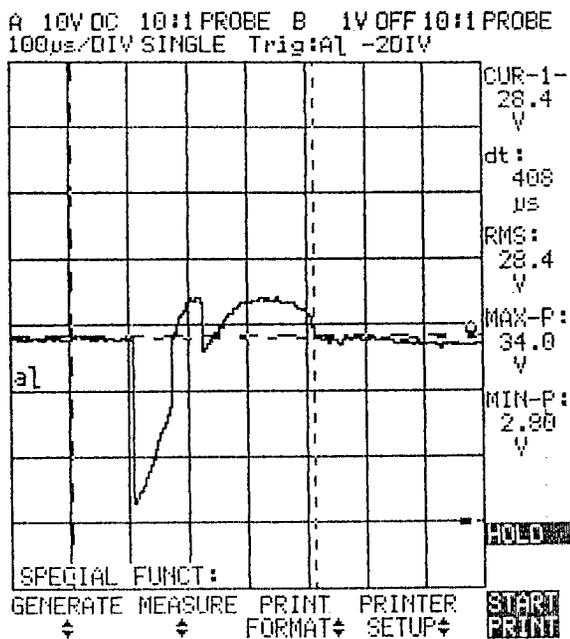


**Oscilloscope A-1:** *Switched near peak*

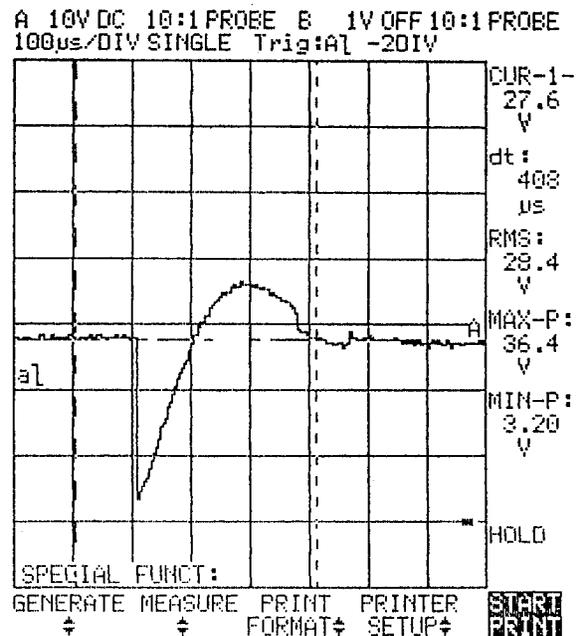


**Oscilloscope A-2:** *Switched near 45°*

Both A-1 and A-2 were generated by FET-switching a 200  $\mu$ F//120  $\Omega$  load on a 60 Hz bus. (Differentiated pulse waveform is external trigger signal.) Test equipment per Appendices D&E.



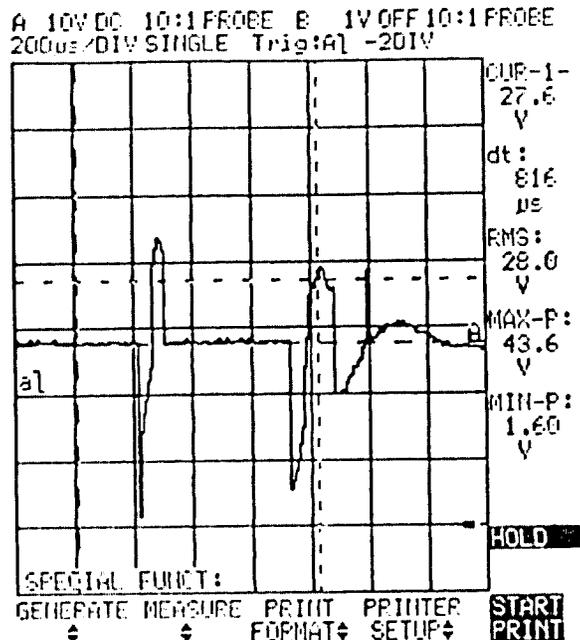
**Oscilloscope A-3:** *Relay switching only*



**Oscilloscope A-4:** *FET switching eliminates bounce*

100  $\mu$ F//11  $\Omega$  switched onto a 28 Vdc bus, using Appendix D test equipment.

## Appendix A: Control of Load-Induced Switching Transient Emission



**Oscillograph A-5:** Same switched load onto 28 Vdc bus as in A-3 and A-4, but using a SPST switch. Bounce is quite evident.

### A3.5.2 TRIGGERING

It is necessary to record waveform such that undisturbed line voltage is displayed before and after transient event. A digital oscilloscope (with required single-event bandwidth) is the most convenient method of capturing waveform. Advantage of a digital oscilloscope for this measurement is in case of triggering. A digital oscilloscope's triggering function is almost opposite in function to that of an analog oscilloscope, in that an analog oscilloscope does not record data until the specified trigger event occurs. The digital oscilloscope, by contrast, can be set to continually record data to memory until trigger event occurs. When the trigger event occurs, the digital oscilloscope ceases to take data once its memory has filled. Thus, data taken prior to trigger event can be recorded, assuring a complete record of transient event leading edge.

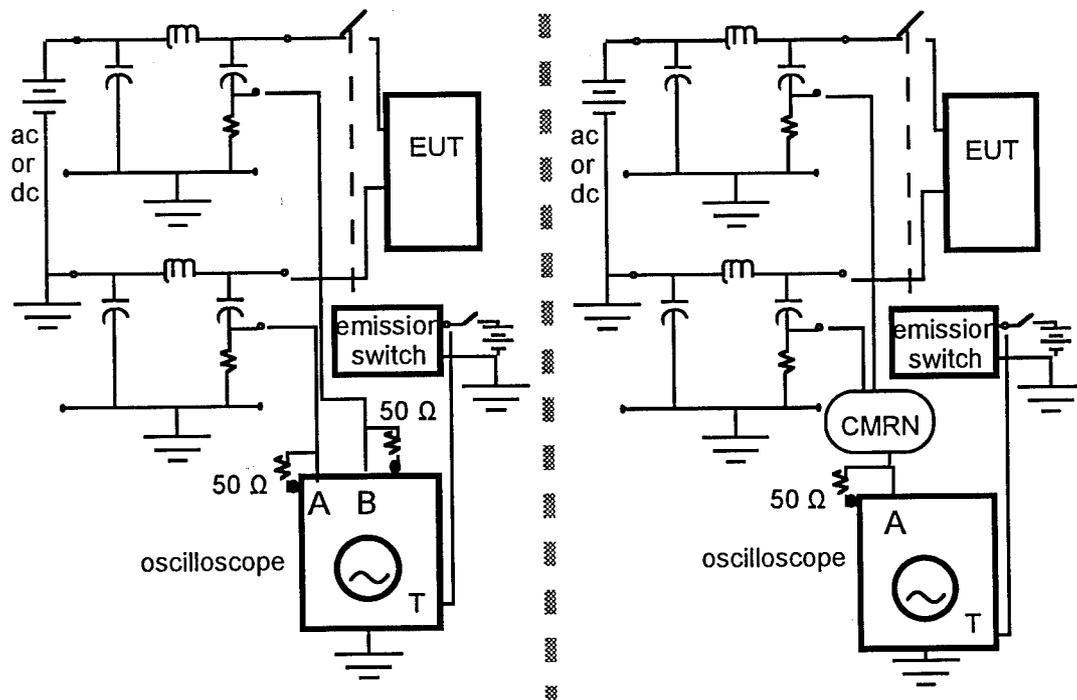
### A3.5.3 TROUBLESHOOTING TEST FAILURES

The following investigation is to be performed in the event of a long duration noncompliance determined when measuring the LISN induced transient. See Figure A3-3 for a representative limit and long duration outage. Dark and dark dashed lines represent limits for turn-off and turn-on transients, respectively, while lighter lines show transient excursions themselves. Shading highlights the area of non-compliance. This procedure exists to facilitate troubleshooting and understanding of test setup. This portion of test verifies that test facility Power Distribution System (PDS) impedance is low enough that transient voltage induced on PDS by cycling EUT on/off or through its modes is negligible relative to specified limit. Purpose is to establish a kind of "ambient" source impedance (as opposed to noise ambients as measured in steady state emission tests) that is

## Appendix A: Control of Load-Induced Switching Transient Emission

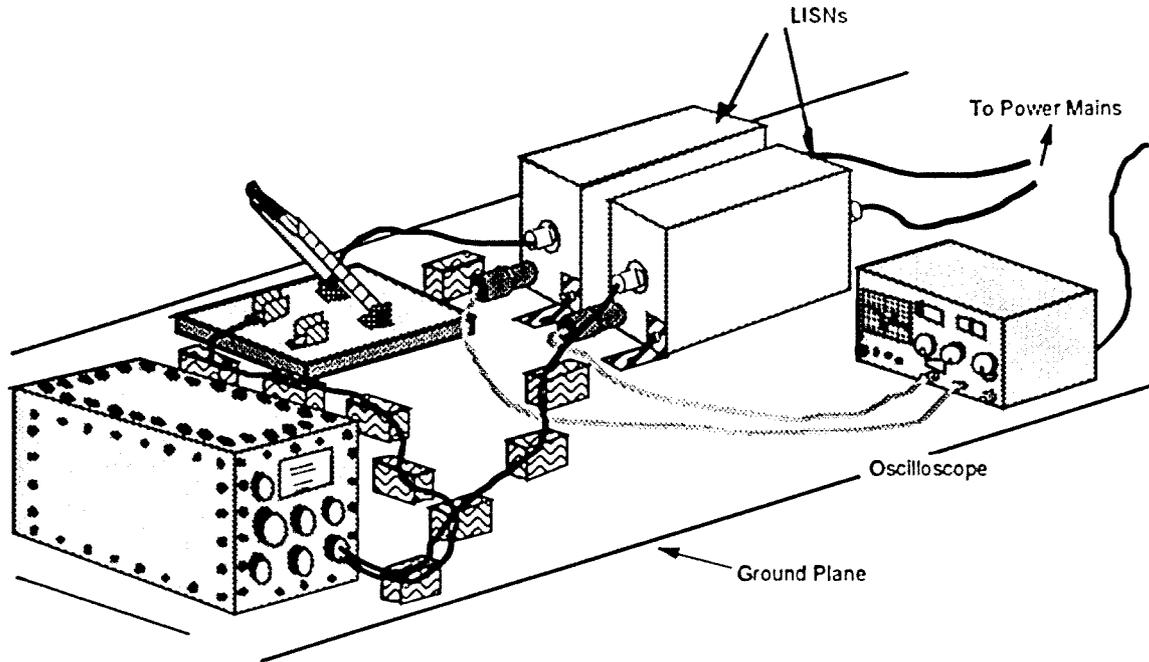
guaranteed not to affect measurement accuracy. This is an "operational" assessment of test facility PDS source impedance: it does not measure impedance directly, but determines whether it is suitable for the EUT in question.

- 1) **Diagnostic Test:** With test setup of Figure A3-4 (which is identical to Figure A3-1, except that 10x probes are connected to input power at each LISN instead of 50  $\Omega$  termination and coax to LISN EMI ports), cycle EUT power on/off and exercise all appropriate mode switches. Record voltage transients. Compare against appropriate transient specification. If any transients are of such magnitude that they materially affect measurement accuracy (specifically, that they cause total transient, PDS induced + LISN induced to be noncompliant) then corrective action must be taken.
- 2) **Lowering the Source Impedance:** A major component of high source impedance in the typical test facility is power line EMI filtering. If a problem is encountered, per A3.5.3 1) above, a possible solution is to use unfiltered power from outside the room. Another possibility is that a regulated power supply is trying to limit or control its output voltage in a manner contributing to transient voltage. Power supply should have a current sourcing capability sufficient to supply EUT inrush current requirements without sagging line voltage below level specified in appropriate power quality document. To lower source impedance of a DC PDS, a simple solution is extra capacitance inserted at PDS input to LISN. This will guarantee that transient is a product of current and LISN impedance only, as is desired.

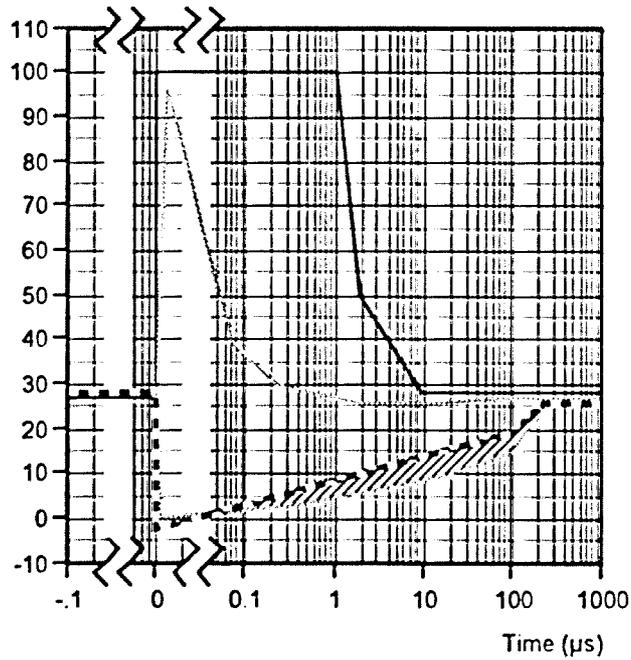


**Figure A3-1:** Schematic of transient test set-up, showing standard and differential measurement techniques

## Appendix A: Control of Load-Induced Switching Transient Emission



**Figure A3-2:** *Transient measurement set-up (relay/oscilloscope trigger and CMRN not shown for simplicity. Switch shown is generic representation only)*



**Figure A3-3:** *Representative limit and long duration outage*

Appendix A: Control of Load-Induced Switching Transient Emission

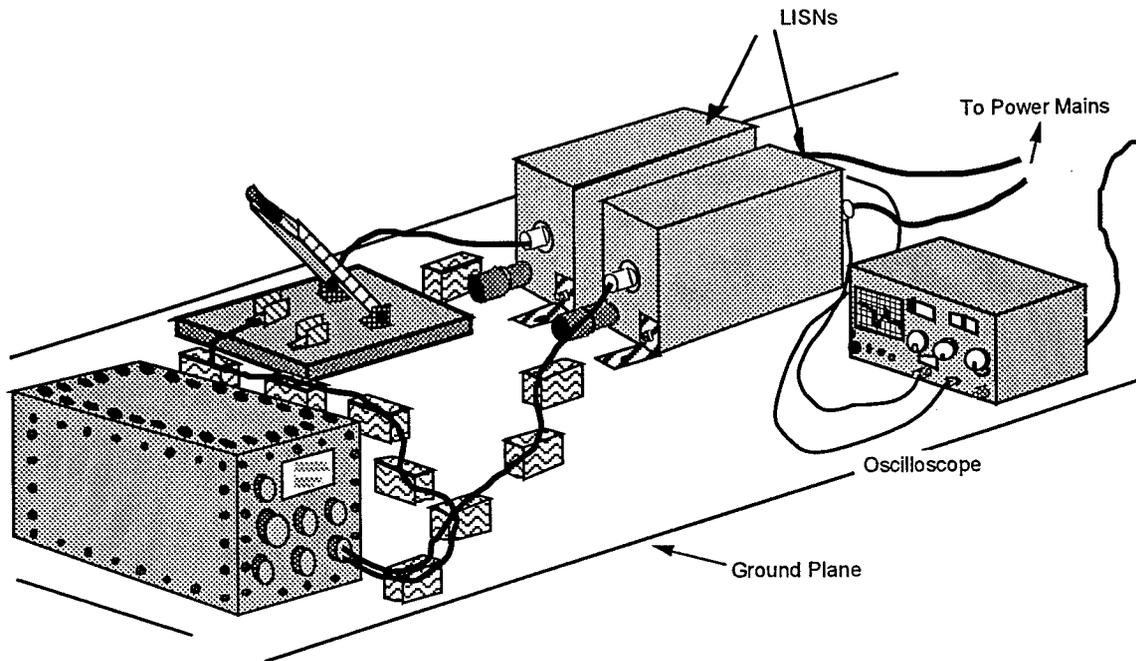


Figure A3-4: Troubleshoot/determination of adequate source impedance

## Appendix B: Control of Inrush Current

### APPENDIX B: CONTROL OF INRUSH CURRENT

#### B1 BACKGROUND AND PHILOSOPHY

The purpose of this test method is to measure, in the time domain, inrush current caused by cycling the EUT on and off, as well as through any and all of its various modes of operation which might reasonably be expected to draw transient currents significantly in excess of steady-state current draw.

Several issues are potentially of interest when cycling loads on/off a power bus. This method addresses inrush current which might excessively load the power source or cause a load to blow its own fuse or circuit protection device. Another issue is rate of change of transient current, which can cause voltage transients due to power bus wiring transmission line characteristics. That issue is addressed under a separate test method.

#### B2 RECOMMENDATION

Because the issue here is transient current draw, this test utilizes a stiff power source and a small resistance across which voltage drop is proportional to current draw. This resistance must be small relative to both EUT transient and steady-state impedance. Power source stiffness must be controlled so that during the entire switching event, including steady-state, voltage measured at EUT power input terminals does not sag more than a percentage of unloaded voltage. This maximum allowable voltage sag is determined as follows.

Power source stiffness is defined as follows. Voltage sag (due to transient inrush current) at power input to test article is less than or equal to the following quantity:

$$\delta V_{\text{transient}} = [V_{\text{nominal}} - V_{\text{minimum}}] \cdot \sqrt{\left(\frac{I_{\text{ss}}}{I_{\text{bus}}}\right)}$$

where,

$\delta V_{\text{transient}}$  = maximum allowable voltage sag during inrush current measurement (V)

$V_{\text{nominal}}$  = power quality specified nominal bus voltage (V)

$V_{\text{minimum}}$  = power quality specified minimum bus voltage (V)

$I_{\text{ss}}$  = test article steady-state current draw (A)

$I_{\text{bus}}$  = power bus maximum steady-state current load (A)

#### B3 JUSTIFICATION

Without control of power source impedance, test data is not repeatable between test sites, and is not guaranteed to represent EUT maximum inrush current.

##### B3.1 REQUIREMENT

Transient inrush current draw shall be limited so that power subsystem is able to maintain voltage levels within power quality specification tolerances and the EUT does not blow its own circuit protection devices. Inrush current control shall only be exerted if power subsystem is current limited enough that individual load cycling can reasonably be

## Appendix B: Control of Inrush Current

expected to result in bus voltage sags, or if bus wiring ampacity is marginal and circuit breakers might open due to excessive transient inrush currents. Inrush current limits shall consider power source stored energy capacity, its capability to supply transient current in excess of its steady-state maximum. This will determine both magnitude and duration of allowable inrush current. Figure B-3.1 illustrates a sample limit. Allowable transient current is normalized to steady-state current draw. The curve is often approximated by a stair-step to ease compliance verification. Inrush current is measured from a stiff source, i.e., one in which power source voltage does not drop significantly when energizing the test article. Test power source shall not simulate the platform power subsystem. The point of the requirement is to control and measure test article transient impedance, thereby controlling power bus transient voltage.

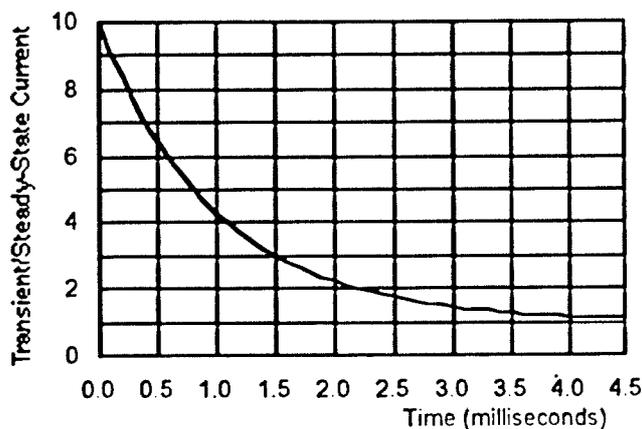


Figure B-3.1: *Transient inrush current sample limit*

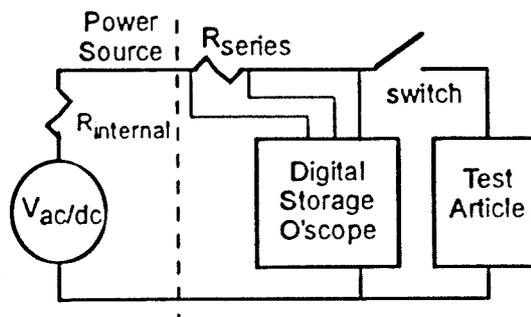


Figure B-3.2: *Transient inrush current test set-up*

### B3.2 APPLICABILITY

Requirement is applicable for measurement of all turn-on and mode-switching transients.

### B3.3 APPARATUS

- Power source, low impedance, as defined under recommendation
- Oscilloscope (1 MHz single event bandwidth)
- Switch (to energize/dc-energize EUT; for ac EUT, switch must turn-on/off at peak of ac waveform). See description under Special Topics.
- Recording Device (to store oscilloscope trace/oscillograph)
- Triggering Device (for analog scopes - triggers oscilloscope from switched EUT power)

### B3.4 TEST PROCEDURE

- Typical test setup is shown in Figure B-3.2.

## Appendix B: Control of Inrush Current

- b. If load operates from an ac bus, then switch must close within 10% of the peak of ac waveform (either polarity is acceptable as long as test article operates as a full wave rectifying load). Sum of internal and series resistance shall accommodate requirement for maximum voltage sag stated above. Bypass capacitance across output of a dc power source can effectively reduce internal resistance.
- c. Prior to measuring inrush current, voltage sag at turn-on shall be measured. Voltage sag shall be in accordance with recommendation section of this test method. If voltage sag does not meet its requirement, power source impedance must be decreased until voltage is compliant.

Source Impedance Calibration: With test setup of Figure B-3.2 cycle EUT power on/off and exercise all appropriate mode switches. Record voltage transients. Compare against appropriate voltage sag limit. If voltage sag is outside limit, take corrective action as below.

Lowering Source Impedance: A major component of high source impedance in a typical test facility is power line EMI filtering and long lines between power source and EUT. A possible solution is to use an unfiltered power source placed adjacent to the EUT. Another possibility is that a regulated power supply is trying to limit or control its output voltage in a manner contributing to transient voltage. Power supply should have a current sourcing capability sufficient to supply EUT inrush current requirements without sagging line voltage below the level specified in the appropriate power quality document. To lower source impedance of a dc bus, place capacitance across the power source.

- d. Cycle EUT power on/off and exercise all appropriate internal EUT mode switches. Record transient current magnitude and duration. Compare against the transient specification.

### B3.5 SPECIAL TOPICS

The following issues are unique to time domain transient tests and are important to their successful measurement.

#### B3.5.1 TIMING OF TURN-ON/OFF EVENT

On ac powered EUTs, it is important to cycle EUT's power near the voltage waveform peak (within 10%) in order to maximize inrush current  $di/dt$ . A special switch, analogous to a zero-crossing switch may be built for this function. The only difference in operation is a 90° phase shift in switching point. Absent such a switch, a lot of data will be taken on a hit or miss basis. A solid state switch is necessary for ac power, since timing must be accurate within  $\pm 1$  ms of a 60 Hz and  $\pm 150$   $\mu$ s of a 400 Hz peak. This switch was developed for this study and is described as to construction and use in the test equipment section. This switch is also used for dc buses, since it does not arc or bounce.

#### B3.5.2 TRIGGERING

It is necessary to record the waveform such that undisturbed current draw is displayed before and after transient event. A digital oscilloscope (with required single-event

## Appendix B: Control of Inrush Current

bandwidth) is most convenient for waveform capture. Advantage of a digital oscilloscope for this measurement lies in ease of triggering. A digital oscilloscope's triggering function is almost opposite in function to that of an analog oscilloscope, in that an analog oscilloscope does not record data until the specified trigger event occurs. The digital oscilloscope, by contrast, can be set to continually record data to memory until trigger event occurs. When trigger event occurs, the digital oscilloscope ceases to take data once its memory has filled. Thus, data taken prior to trigger event can be recorded, assuring a complete record of transient event leading edge.

## APPENDIX C: CONTROL OF IMMUNITY TO POWER-LINE SWITCHING TRANSIENTS

### C1 BACKGROUND AND PHILOSOPHY

The purpose of this test method is to measure, in the time domain, EUT susceptibility to positive and negative spikes superimposed on EUT-input power lines. Such spikes are representative of typical load-induced switching transients on a power bus.

Traditional spike susceptibility waveforms are symmetric with respect to polarity. That is, whether the spike has a positive or negative polarity with respect to the nominal power bus potential, the waveform shape is identical. Since this requirement models switching transients, this is not true for the spikes imposed herein. The spikes are induced by switching an RC load from a source impedance shared by the EUT, namely a LISN. When the RC load is switched on, the bus potential sags and then recovers, typically over a period of 10s to 100s of microseconds, and the sag never dips the bus potential below zero. When the load is switched off, the bus potential increases to a potential which is the product of the switched current and the LISN impedance, for a duration related to the quotient of the LISN inductance by its EMI port resistance. This duration is typically microsecond or sub microsecond.

### C2 RECOMMENDATION

It is important that the RC load be switched on and off the bus in a precise and repeatable manner. This means a solid-state switch. If the EUT is powered from an ac bus, it is further important to synchronize the spike with ac waveform phase (and to be able to vary that phase synchronization). Test equipment providing this capability is described elsewhere in this report.

It is important to use a LISN which is either representative of the *in situ* EUT power bus, or a reasonable worst case simulation. If two LISNs are used, each with an EMI port terminated in a resistance (usually 50  $\Omega$ ), then the differential source impedance is twice this EMI port resistance.

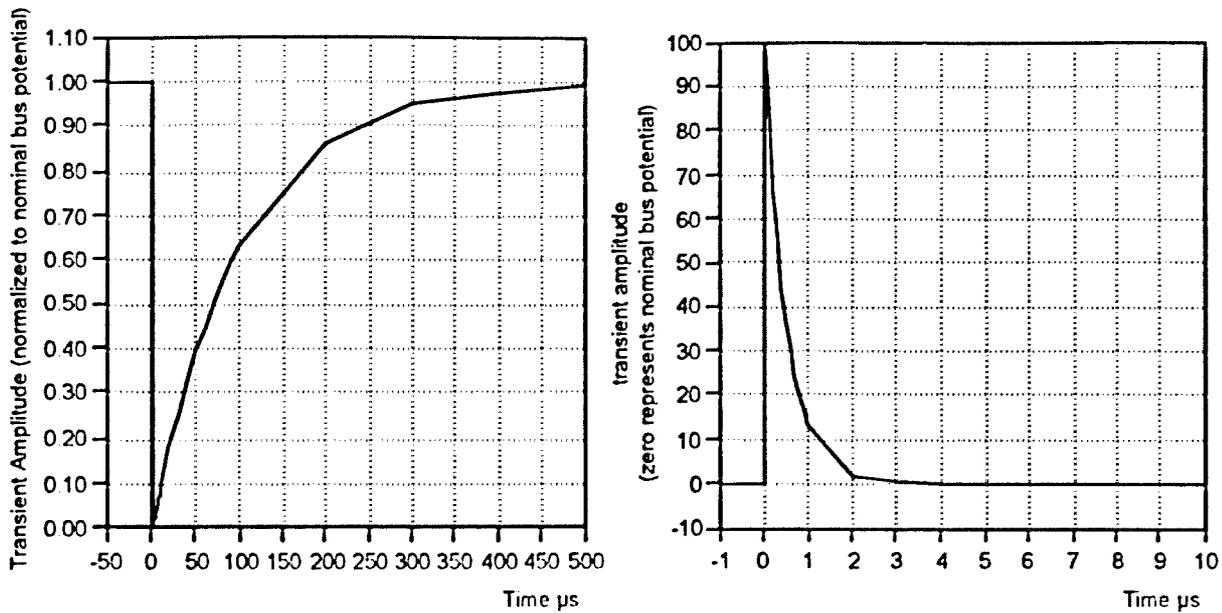
### C3 JUSTIFICATION

Without control of both switching rise and fall times, and LISN impedance, an uncontrolled test results.

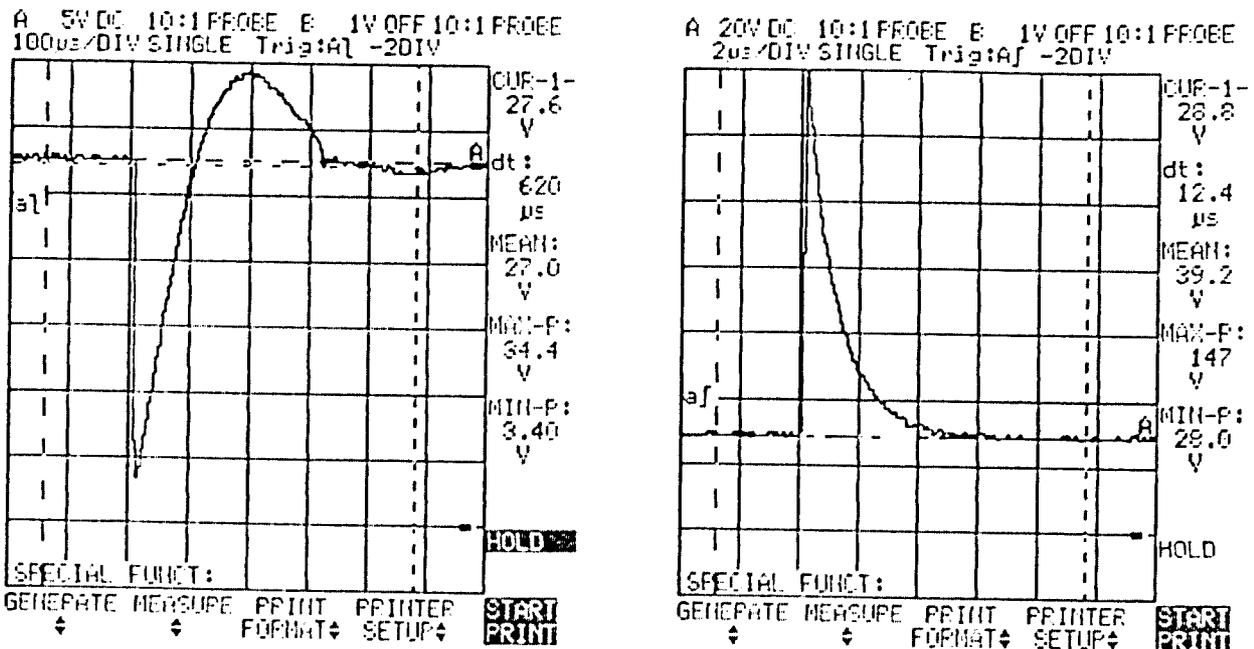
#### C3.1 REQUIREMENT

Susceptibility to switching transients shall be controlled such that the EUT is immune to typical or reasonable worst case normal switching transients likely to be induced on the power bus. The amplitude and duration of such transients can be estimated from the magnitude of likely bus switched currents, the LISN model of the power bus, and estimates of hold-up capacitance associated with a given current draw (so many microFarads per Amp). Figure C-3.1 shows typical waveforms. Test data in oscillographs C-1 and C-2 depicts susceptibility spikes generated by test equipment described in Appendix E.

## Appendix C: Control of Immunity to Power-Line Switching Transients



**Figure C-3.1:** *Transient susceptibility waveforms*



**Oscillograph C-1:**  $10\Omega//100\ \mu F$  load switched on-line      **Oscillograph C-2:**  $10\Omega//100\ \mu F$  load switched off-line

Both of the loads in oscillographs C-1 and C-2 are switched from a 28 Vdc bus with a single line-to-ground configuration  $50\ \mu H$ ,  $50\ \Omega$  LISN as source impedance.

### C3.2 APPLICABILITY

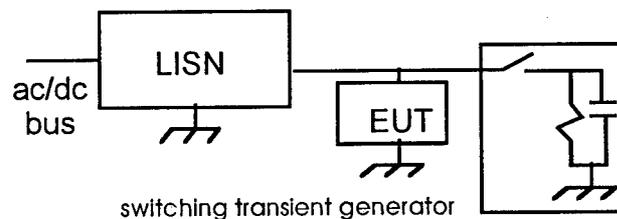
Requirement is applicable for the determination of susceptibility to all switching transients.

### C3.3 APPARATUS

- a. LISN
- b. Oscilloscope (10 MHz single event bandwidth)
- c. Switching transient generator. See description under Special Topics.
- d. Recording Device (to store oscilloscope trace/oscillograph)
- e. Triggering Device (for analog scopes - triggers oscilloscope from switched EUT power)

### C3.4 TEST PROCEDURE

- a. Typical test setup is shown in Figure C-3.2.



**Figure C-3.2:** *Transient susceptibility test set-up*

- b. If EUT operates from an ac bus, then transient generator must be phase selective and be able to close switch within 10% of the peak of ac waveform (with both ac waveform polarities being separately selectable).
- c. Transients should be measured open circuit (using an oscilloscope) with the EUT de-energized. The EUT will load the transient (especially the turn-off or positive-going transient). Specification level transients must be established open circuit prior to EUT power up. Transient waveform as applied to the EUT is of informational value only.
- d. In order to measure transients on ac bus, a separate external trigger source is necessary. The switching transient generator circuit should provide this source.
- e. Energize EUT and verify proper operation. Apply all the following spikes at a rate of 1 -10 pps. Switching transient generator should also be capable of providing a single pulse to assist evaluation of EUT response.
  - 1) turn-on (negative polarity wrt nominal power bus potential). On an ac bus, this spike should be applied within 10% of the ac waveform peak, and at 45°. The turn-on spike should be applied to each ac waveform polarity. So there are four ac waveform turn-on tests: 45° and near 90° on both polarities of the ac bus potential.

## Appendix C: Control of Immunity to Power-Line Switching Transients

2) turn-off (positive polarity wrt nominal power bus potential). On an ac bus, this spike should be applied within 10% of the ac waveform peak, and at 45°. The turn-off spike should be applied to each ac waveform polarity. So there are four ac waveform turn-off tests: 45° and near 90° on both polarities of the ac bus potential.

3) It may be desirable to impose a sequence of turn-on and turn-off transients. Again, on an ac bus, these must be applied at 45° and 90°, and on each ac waveform polarity sequentially.

- f. Monitor EUT for susceptibility during all spike application. Duration of spike application is EUT dependent.

### C3.5 SPECIAL TOPICS

The following issues are unique to time domain transient tests and are important to their successful measurement.

#### C3.5.1 TIMING OF TURN-ON/OFF EVENT

On ac powered EUTs, it is important to generate the switching transient near the peak (within 10%) of voltage waveform in order to maximize switched current absolute magnitude and di/dt. A special transient generating switch, may be built for this function. A solid state switch is necessary for ac power, since timing must be accurate within  $\pm 1$  ms of a 60 Hz and  $\pm 150$   $\mu$ s of a 400 Hz peak. Such a switching transient generator was developed for this study and is described as to construction and use in the test equipment section. This switch is also used for dc buses, since it does not arc or bounce and provides the nanosecond rise-/fall-times necessary to get repeatable waveforms.

#### C3.5.2 TRIGGERING

It is necessary to record the transient waveform such that undisturbed bus potential is displayed before and after transient event. A digital oscilloscope (with required single-event bandwidth) is most convenient for waveform capture. Advantage of a digital oscilloscope for this measurement lies in ease of triggering. A digital oscilloscope's triggering function is almost opposite in function to that of an analog oscilloscope, in that an analog oscilloscope does not record data until the specified trigger event occurs. The digital oscilloscope, by contrast, can be set to continually record data to memory until trigger event occurs. When trigger event occurs, the digital oscilloscope ceases to take data once its memory has filled. Thus, data taken prior to trigger event can be recorded, assuring a complete record of transient event leading edge.

APPENDIX D: PRECISION PHASE-CONTROLLED POWER SWITCH DESCRIPTION

D1. PURPOSE

The Precision Phase-Controlled Power Switch (emission switch, for short) provides a capability to precisely and accurately energize any power bus load from 28 Volts to 270 Volts, ac or dc. Precision and accuracy mean that the turn-on transient will always be the same waveform and occur (for an ac bus) at the phase commanded. The emission switch utilizes a LISN as a source impedance between power source and EUT. See Figure D-1. The emission switch itself is actually comprised of four sub units and an interface cable. One sub unit is the control unit, and there are three identical form, fit and function power switching units designated PSU-28, PSU, 120, and PSU 270. The number designators relate to the typical power bus potential the switch was designed for. Actual peak values of usage for each PSU is red-stenciled on each chassis and is explained below.



Figure D-1: Emission switch test setup

D2. DESCRIPTION OF OPERATION

The emission switch uses a FET to energize the EUT with sub-microsecond risetime. Further, an ac sync function allows the user to select any phase between 0 and 90 degrees at which to turn on. (The turn-off point is also at the same phase).

D2.1 SELECTION OF CORRECT FET VALUES

There is an exponential relationship between maximum FET drain-to-source potential and on resistance. The higher the allowable drain-to-source potential, the higher the on resistance. For instance, a FET rated at 70 Volts drain-to-source potential with an on resistance of 6 mΩ was chosen for use switching 28 Vdc. A similar technology FET used to switch 270 Vdc is rated at 500 Volts drain-to-source potential and 0.2 Ω on resistance. Given that the on resistance of the switch should be small relative to the expected dc resistance of the power bus, it is impossible to simply use a single high potential FET. A 28 Vdc bus will often have source resistance of 10 mΩ or less. Increasing that resistance significantly has the effect of stretching out the turn-on transient. As bus potential increases, so does source resistance, since wire resistance is allowed to rise. So a selection of FETs are used:

- For bus potentials up to 40 Vdc or 28 Vrms, a 70 Volt FET with 6 mΩ on resistance was selected. Typical bus in this range is 28 Vdc. (PSU-28)
- For bus potentials between 40 Vdc/28 Vrms and 140 Vdc or 100 Vrms, a 200 Volt FET with 20 mΩ on resistance was selected. Typical bus potentials in this range are 120 Vdc, (Space Station). If the user is careful to only measure turn-on and NOT turn-off transients, then this unit can also be used to switch loads on (clean) 120 Vrms (60 Hz) power. (PSU-120)

## Appendix D: Precision Phase-Controlled Power Switch Description

- For bus potentials above these levels, but below 300 Vdc or 210 Vrms, a 500 Volt FET with  $0.2 \Omega$  on resistance was selected. Typical bus potentials in this range are 120/220 Vac, 50/60 or 400 Hz, and 270 Vdc. (PSU-270)

### D2.2 SETUP

#### WARNING!

When connecting an oscilloscope across a power bus, precautions must be made. Never connect neutral or return to a conventional scope ground unless that return or neutral is chassis grounded on the EUT side of the LISN. If the scope itself has a floating ground (this last highly recommended for this type of measurement) then that ground can be connected to any portion of the test setup. Also, regardless of whether the scope has a floating ground or not, no other connection from the scope to anywhere should be made except (when necessary, as described below) the "AC TRIGGER OUT" may be connected to the other channel.

Having chosen the appropriate switching head the emission switch may now be integrated into the test setup, which is now redrawn as Figure D-2. Also please refer to photos of test equipment at end of this appendix. A connection from the LISN phase or high potential feeder is made to a recessed male connector in the switching head (labeled "FROM LISN"). The switched output from the switching head is labeled "TO EUT". Neutral or return is carried directly from the LISN or ground to the EUT neutral or ground power connection. The control cable connects to the opposite side of the switching head. If the bus potential is ac, provide a clean source of ac power to the back panel terminals of the control unit so labeled. Clean power means that if the LISN is fed from filtered power within a shielded/screened enclosure, the ac sync source should originate outside the room, so that the entire attenuation associated with the room filtering is available to attenuate the induced spike form the sync source. Otherwise, the measured emission will be noisy and jittery. The control cable also connects to the control unit back panel. Emission switch ac power is also applied to the back panel.

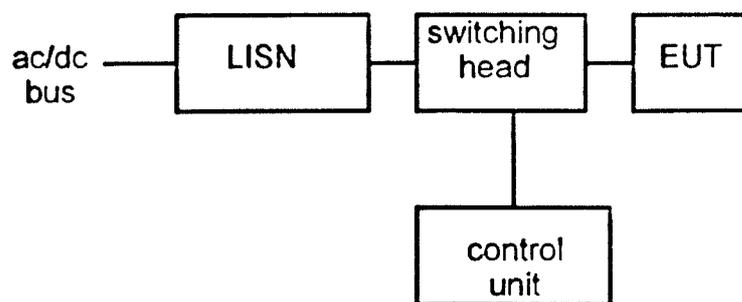


Figure D-2: Transient emission measurement setup

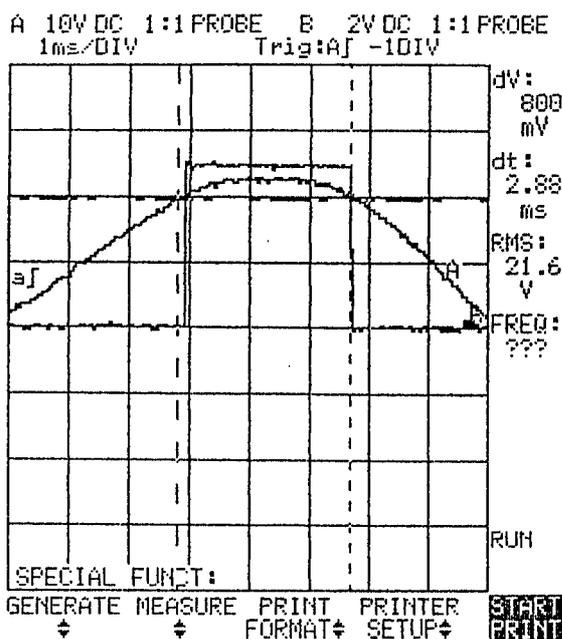
### D2.3 OPERATION

Once setup is complete, emission switch front panel controls may be properly adjusted. Operation on a dc bus is simpler, it is described first. The "BUS" switch should be set to "DC". "PHASE ANGLE" only applies to ac buses. The large knob labeled "EUT" applies/removes power to the EUT. The "ENGAGE FOR TURN-ON TRANSIENT" momentary on switch connects the FET in parallel with a relay which switches power. Unless the "ENGAGE" switch

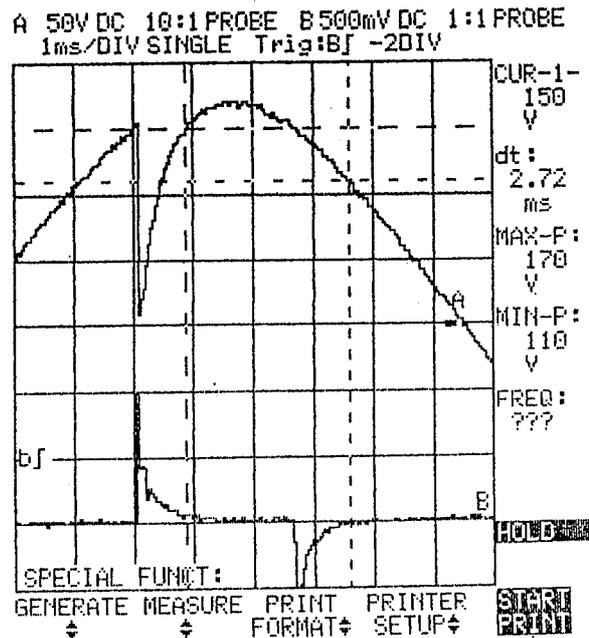
## Appendix D: Precision Phase-Controlled Power Switch Description

is held in prior to the EUT ON/OFF switch changing state, ONLY A RELAY WILL SWITCH POWER. This is to protect the FET. It is STRONGLY ADVISED only to depress the "ENGAGE" switch for turn-on, not turn-off transients. The switching heads are all designed to switch 20 Amps. If 20 Amps were switched from a 50  $\Omega$  LISN, a 1000 Volt transient would be developed, which would likely damage the FET. It is easy to record the transient, even though it is a short duration, low duty cycle phenomenon. Use a digital oscilloscope (10 MHz single-event bandwidth - Nyquist criteria - is sufficient). Trigger on a level either above or below nominal with suitable slope as appropriate. Use a time per division near the expected transient duration. This will be on the order of 100  $\mu$ s/division.

If the EUT runs off an ac bus, the following extra settings must be adjusted. The "BUS" switch must be set to "AC", as applicable. Phase angle (at what point along the ac waveform switching is to occur) is selected as follows. Connect "AC reference" to oscilloscope channel A. Connect "PHASE ANGLE MONITOR" to channel B. Adjust "PHASE ANGLE" knob until channel B rectangular waveform leading and falling edges intercept desired phase point along channel A rectified ac waveform. Test data in oscillographs D-1 and D-2 illustrate the technique.



**Oscilloscope D-1:** *Ac reference and phase adjustment*



**Oscilloscope D-2:** *Actual switched ac bus and isolated trigger signal used to capture it*

When trying to record a transient on the ac bus, a special external trigger "AC TRIGGER OUT" must be used. Connect Channel B to this port. Set the trigger to Channel B, with trigger point about 0.5 Volt. Select a positive 0.5 Volt and positive slope for recording a turn-on transient, and a negative 0.5 Volt and a negative slope when recording a turn-off transient. The AC TRIGGER OUT is isolated from chassis, so the ac bus ground scheme is not compromised.

### D3. PRECISION PHASE-CONTROLLED POWER SWITCH CIRCUIT DESCRIPTION

Please refer to the enclosed schematic (Figure D-3) to follow the description.

Two low voltage power supplies are utilized. These develop 5 Vdc and 12 Vdc. 5 Vdc is referenced to chassis ground. 12 Vdc is referenced to the low side of the rectified bus potential. This 12 Volts is used to drive the actual switching elements which must be referenced to the low side of the (rectified) EUT power bus. For this reason, NEVER OPERATE EMISSION SWITCH WITH LID OFF. DANGEROUS POTENTIALS EXIST, NOT ONLY AT AC TRANSFORMER INPUTS AND AC SYNC, WHERE EXPECTED, BUT ALSO ALL 12 VDC CIRCUITS. For instance, if the EUT bus were 270 Vdc, the 12 Vdc reference would be 270 Vdc, and 12 Vdc would actually be at 282 Vdc.

An AC sync circuit generates a 5 Vdc pulse whose leading and trailing edges line up with the desired switching point along the ac waveform. A clean source of ac power is applied to the input transformer. Rectifier output gets fed (through a 10 k $\Omega$  current limiter) to the front panel BNC connector labeled "AC REFERENCE". It also is fed to a resistive divider made up in part of a front panel 5 k $\Omega$  audio taper pot labeled "PHASE ANGLE". This pot adjusts base drive into a switching transistor. To get proper polarity, a second switching transistor is configured as an inverter. The output of this second stage is fed into the next circuit via the front panel DPDT switch labeled "BUS". It is also fed to a front panel BNC connector labeled "PHASE ANGLE MONITOR" via a 10 k $\Omega$  current limiter.

The next portion of the circuit provides for ac synchronized turn on and turn-off. A flip flop is used to hold the EUT on even after the conditions for turn on have ceased. Either the ac sync output pulse or 5 Vdc is selected via the front panel "BUS" switch to connect to pins 1& 13 of a 4011 quad two-input NAND gate. The other inputs to these gates (pins 2&12) are either 5 Vdc and ground (turn-on) or ground and 5 Vdc (turn-off). The 5 Vdc and ground are fed from a front panel 4PDT switch labeled "EUT". These dc signals are fed into the gates via a series 1 k $\Omega$  and shunt 10  $\mu$ F cap to yield a 10 ms delay. Gate outputs (pins 3&11) feed a 74HCT74 flip flop. Pin 3 feeds the RESET pin 1, and pin 11 feeds the SET pin 4. Q and Q outputs are available on the 7474 pins 5&6. One of these outputs drives a front panel LED through a switching transistor buffer, and also drives an opto-isolator via a 510  $\Omega$  current limiting resistor.

The same 4PDT switch which routes 5 Vdc and ground into the 4011 also routes 12 Vdc and ground in exactly the same manner to the coil of a (control unit) DPDT relay. When the relay coil is energized, ground is connected to the base of a transistor which in turn opens the coil of a (switching unit) NO relay in the switching unit. This removes power from the EUT. Because of the 10 ms delay built into the 4011 input, this relay opens before the FET, allowing, if desired, the FET to de-energize the EUT (yielding the accurate and precise turn-off waveform). When the 4PDT switch is reversed, the (control unit) relay opens and the transistor base is no longer shorted to ground. Further, 12 Vdc is applied through a series 1 k $\Omega$  and shunt 22  $\mu$ F to the same transistor base. This implements a 22 ms delay in turning on the transistor and hence energizing the coil of the (control unit) NO relay. This applies power to the EUT. Since the 22 ms delay is longer than the 10 ms delay in the FET circuit, the relay closes after the FET, allowing the FET to establish the precise and accurate turn-on waveform, but allowing the relay to carry the steady-state current. This obviates any need to heat sink the FET.

## Appendix D: Precision Phase-Controlled Power Switch Description

The opto-isolator output drives two parallel IR2121 FET drivers. These circuits allow fast turn-on/off of the FET. The FET drain is connected via a relay to the "+" output of a 25 Amp, 600 Volt rectifier bridge whose ac inputs connect to the switching unit LISN input and EUT output. The source is connected to the low side of the rectified bus potential. When the switching FET is turned on, the dc bridge outputs are connected and ac/dc current can flow through the bridge. When the FET is turned off, the circuit is broken. The control unit front panel momentary on "ENGAGE" switch grounds one side of the series relay allowing the FET to be in parallel with the shunt relay.

### D3.1 PARTS DESCRIPTION

All resistors are quarter Watt. All transistors are general purpose switching transistors. The PCB was laid out single-sided. This made for easy board fabrication, but messy board I/O. A two-sided approach is recommended, with I/O run out to edge connections on second side. Power supply rectifier bridges are 6 pin DIP packages with four pins.

With the following exceptions, all circuit components are available at Radio Shack. The exceptions are:

- power FETs: IXYS
  - IXFN48N50-ND (500 Volt, 48 Amp)
  - IXFN106N20-ND (200 Volt, 106 Amp)
  - IXFN200N07-ND (70 Volt, 200 Amp)
- FET drivers: International Rectifier IR2121
- opto-isolators: NTE 3090
- switches more complex than DPDT
- 25 Amp NO relays, PCB mount style
- 25 A, 600 Volt EUT power bus full-wave rectifier bridge
- Isolated bnc feedthrough connector

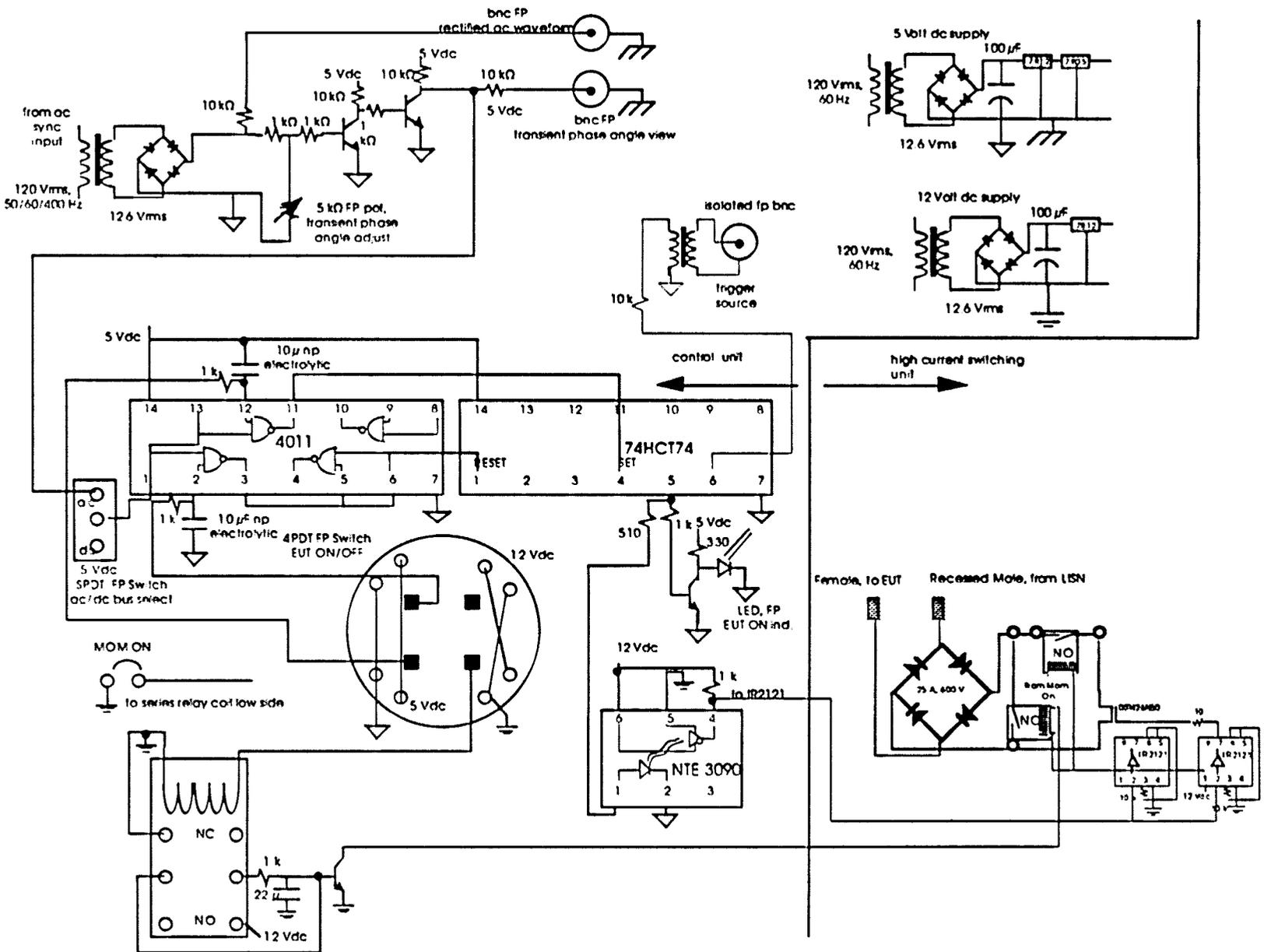


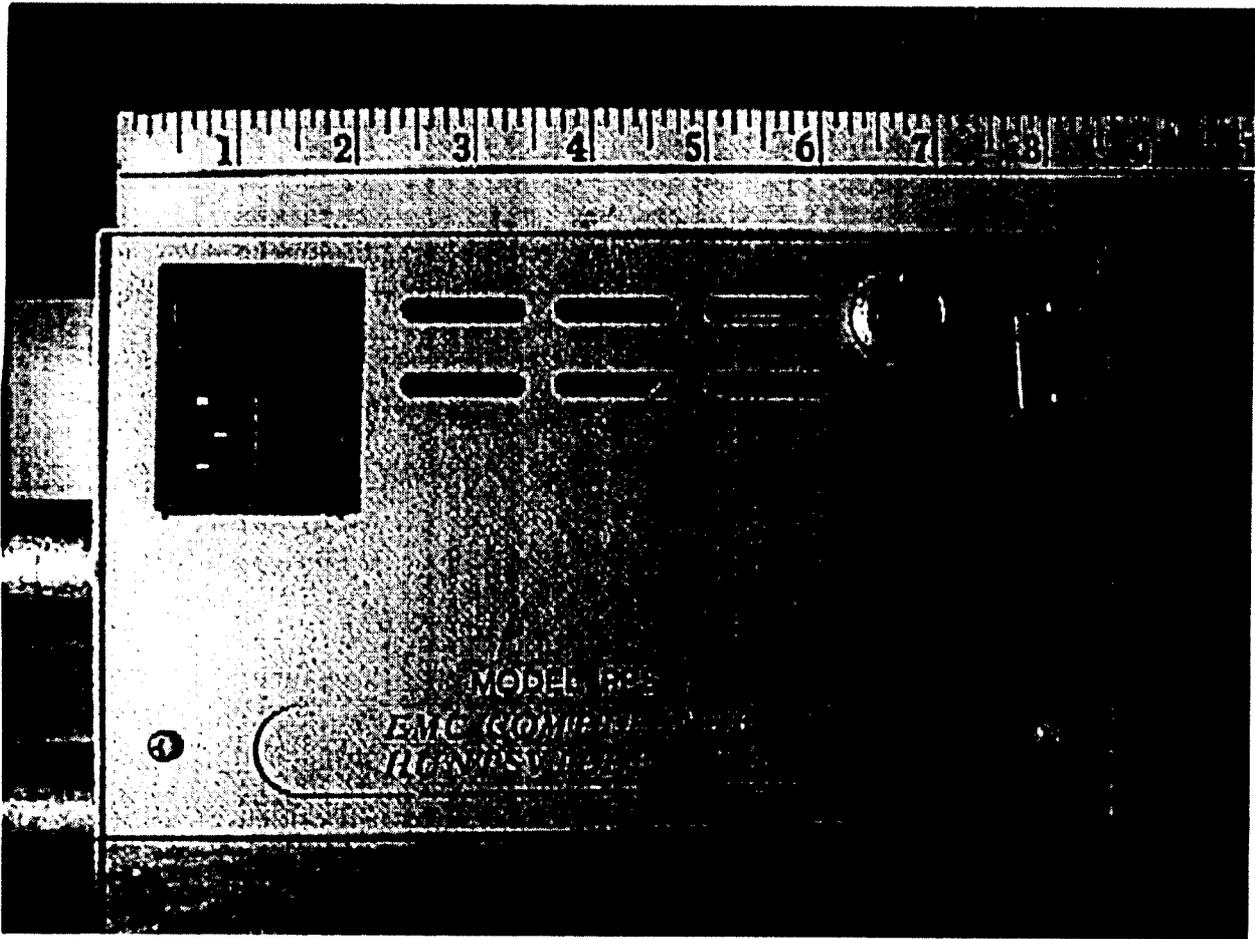
Figure D-3: Functional Schematic of Precision Phase-Controlled Power Switch

Appendix D: Precision Phase-Controlled Power Switch Description



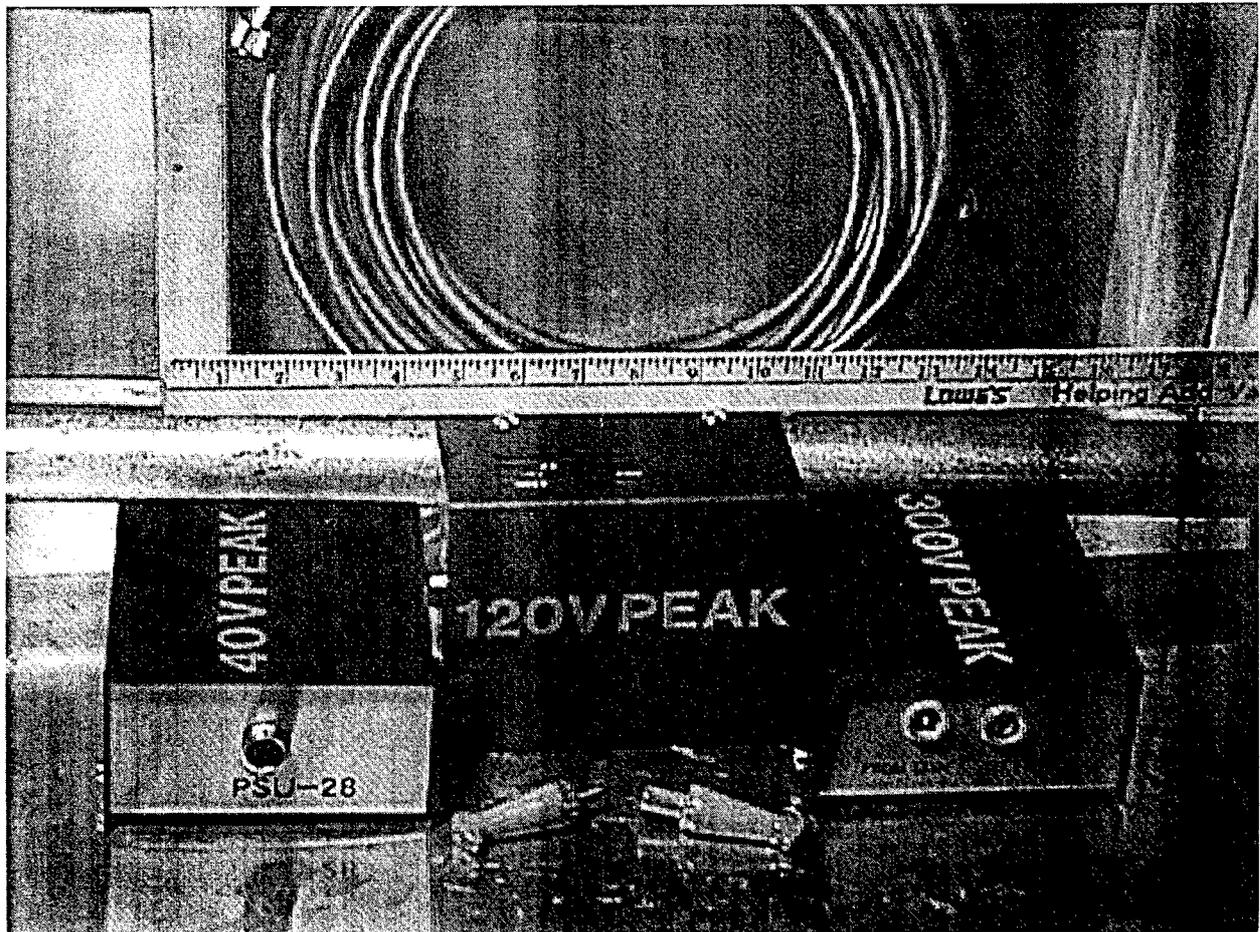
**Plate D-1:** Front panel of Precision Phase-Controlled AC/DC Power Switch, designated here-in as Emission Switch.

Appendix D: Precision Phase-Controlled Power Switch Description



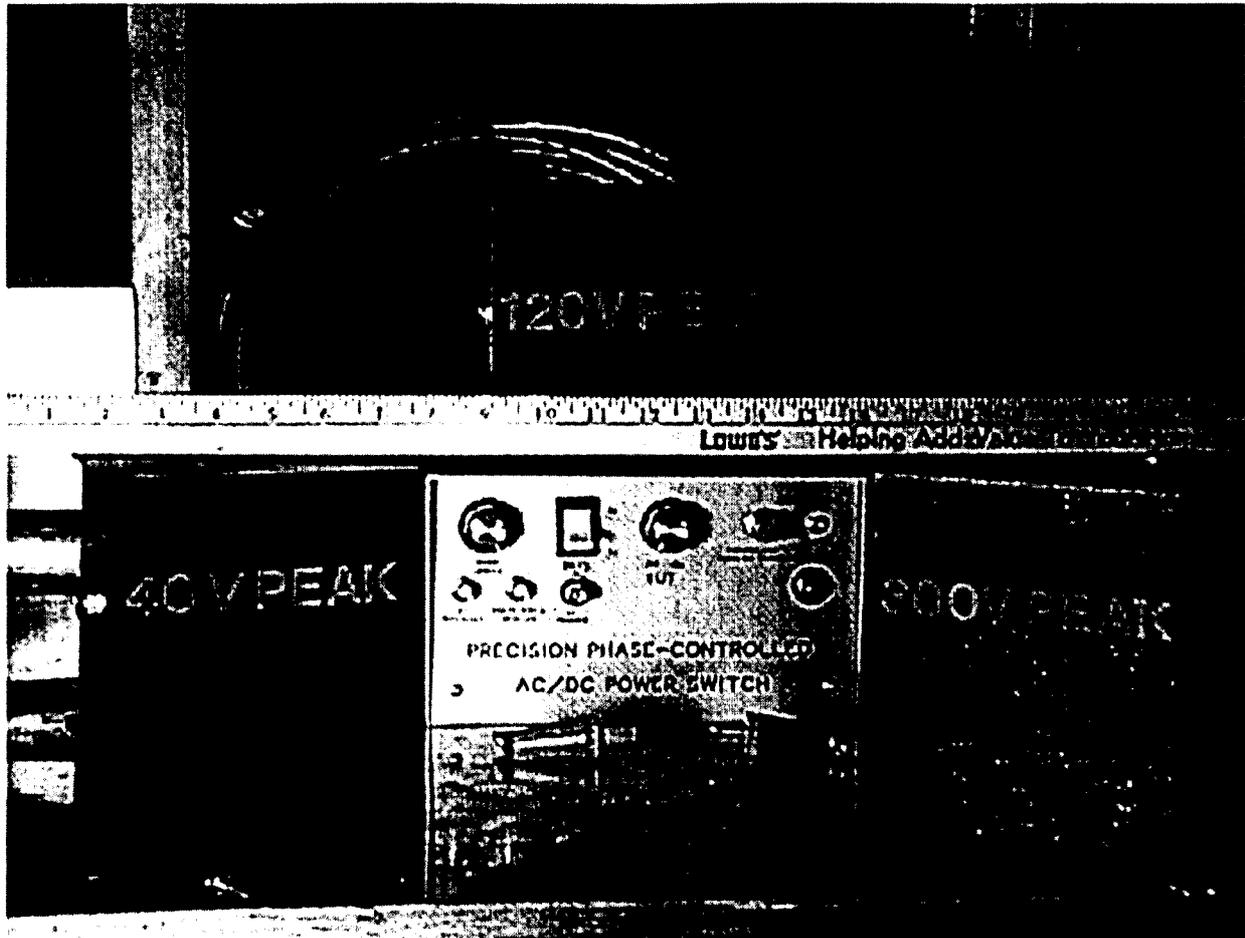
**Plate D-2:** *Rear panel of Precision Phase-Controlled AC/DC Power Switch, designated here-in as Emission Switch.*

Appendix D: Precision Phase-Controlled Power Switch Description



**Plate D-3:** *Three switching heads, designated PSU-28, PSU-120, and PSU-270. In the background the 40' control unit/power switching unit interface cable is visible. In the foreground the 25 Amp power connectors rest on the ground plane.*

Appendix D: Precision Phase-Controlled Power Switch Description



**Plate D-4:** *The entire emission switch system: control unit, switching heads, interface cable and 25 Amp power connectors.*

APPENDIX E: SWITCHING TRANSIENT GENERATOR DESCRIPTION

E1. PURPOSE

The STS-1 (Switching Transient Simulator) injects simulated switching transients between power feeders supplying the EUT. The STS-1 utilizes a LISN as a common source impedance between power source and STS-1 and EUT. See Figure E-1.

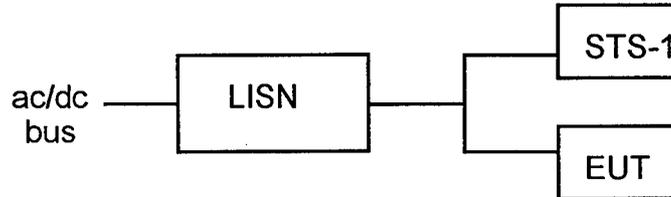


Figure E-1: STS test setup

E2. DESCRIPTION OF OPERATION

STS-1 switches a user selectable resistor/capacitor (RC) load on and off the power bus in an accurate repeatable fashion. The RC combination is chosen to yield power quality or EMI specification transient envelopes.

E2.1 SELECTION OF RC VALUES

The R value will be representative of the worst case load which might be rapidly switched off the bus. A bound on this value is a 500 Volt turn-off transient amplitude (including nominal bus potential). (This is the STS-1 switching FET rating. Rating is conservative because the transient is microsecond duration.) The C value will be that which yields a suitable safety margin above a reasonable hold-up time constant in parallel with the chosen R value. Figure E-2 represents a typical such specification for switching transients (except that it realistically portrays the positive transient rather than making it the mirror image of the turn-on transient.)

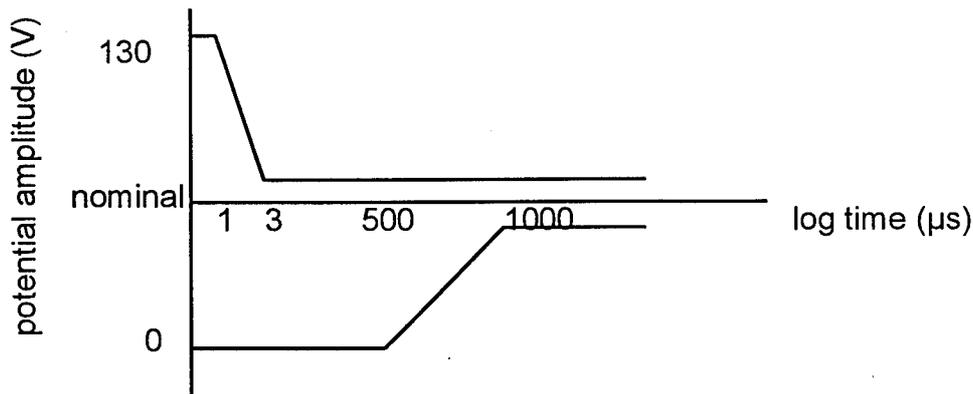


Figure E-2: Representative switching transient envelope specification.

The R value is defined (ignoring safety margin) by the high frequency impedance of the LISN (typically either 50 Ω or 100 Ω) multiplied by the current drawn by the R value. This must equal the positive excursion value. For example, if the bus is 28 Vdc and LISN in question has a 50 Ω high frequency asymptote, the switched current must, when multiplied by 50 Ω, yield 100 Volts (130 Volt total excursion - nominal 28 Vdc). So the switched current must be 2 Amps, and

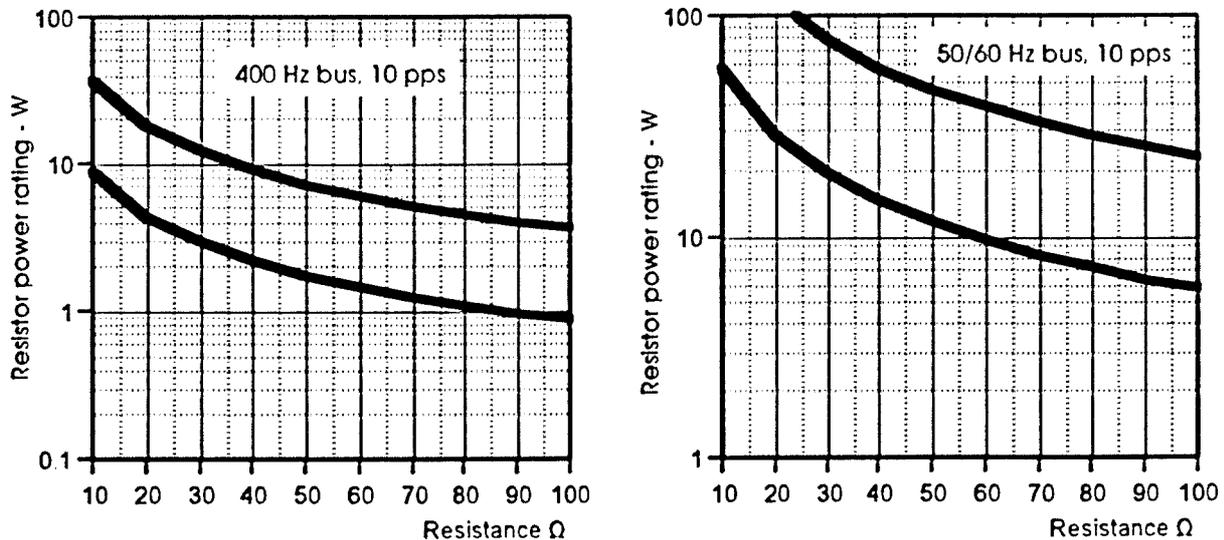
## Appendix E: Switching Transient Generator Description

the R value is then  $28 \text{ Vdc}/2 \text{ Amps} = 14 \Omega$ . A 6 dB safety margin (yielding a 230 Volt spike) would be achieved by using a  $7 \Omega$  resistance. (Note that the safety margin was calculated wrt the transient amplitude alone, ignoring the nominal bus potential. This is reasonable for 28 Vdc. It is not reasonable at higher bus potentials.) Note further that for the positive spike, a safety margin can only be achieved by increasing the spike potential. Time duration can only be affected by varying LISN properties (L/R ratio for LISN components). The  $1 \mu\text{s}$  time constant of the positive going transient is provided by a LISN whose L/R ratio is  $1 \mu\text{s}$ , such as is the case with a  $50 \mu\text{H}$ ,  $50 \Omega$  LISN, or two of these, one in each power feeder, yielding a  $100 \mu\text{H}$ ,  $100 \Omega$  differential mode LISN impedance. A Space Station LISN with  $L = 20 \mu\text{H}$ , and  $50 \Omega$  high frequency asymptote would yield a shorter time constant of  $0.4 \mu\text{s}$ . The Shuttle LISN would yield a  $8 \mu\text{H}/50 \Omega = 0.16 \mu\text{s}$  spike.

A note about the switched load resistor power rating: Due to low duty cycle, it can be considerably derated. The STS-1 is designed to provide the following pulse widths, and repetitions rates:

power bus	pulse width (ms)	min pps	max recommended pps	derating factor @ 10 pps
dc	1	< 1	10	100
50/60 Hz	2 - 8	< 1	10	50 - 12.5
400 Hz	0.3 - 1.25	< 1	10	330 - 80

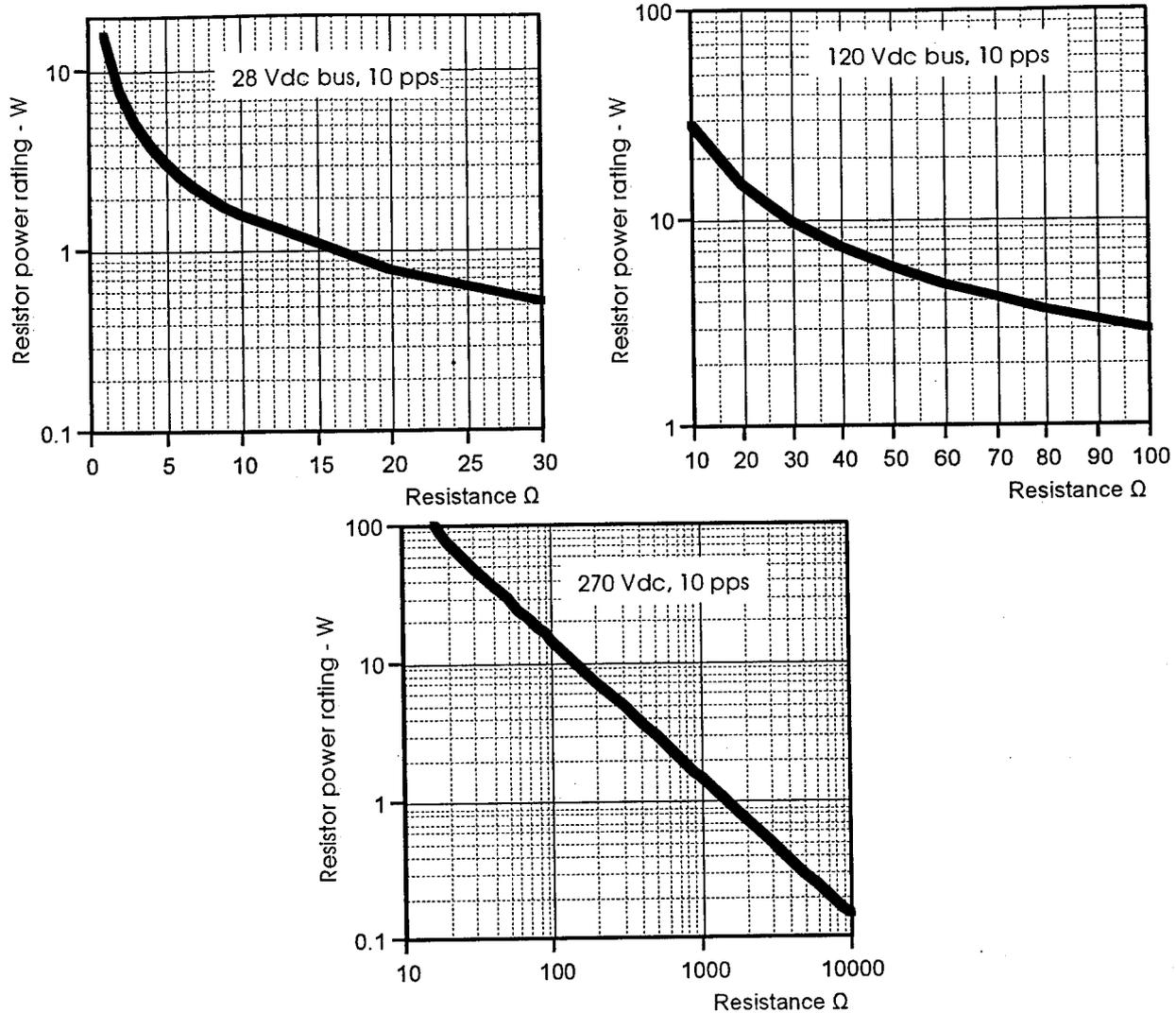
Using the above example of a  $7 \Omega$  resistor operating from a 28 Vdc bus, the derating factor is 100. Full power dissipated by the  $7 \Omega$  resistor would be 112 W. So the  $7 \Omega$  resistor should have at least a 2 W rating to remain reasonably cool. Figures E-3 through E-4 present results of similar calculations.



**Figure E-3:** Resistor power derating for ac buses. Upper band limit represents on-time of 1/2 ac cycle. Lower limit represents cycling on/off near peak of ac waveform (2 ms for 50/60 Hz, 300  $\mu\text{s}$  for 400 Hz bus).

[A single pulse capability, if desired, is easily achieved. Turn PPS knob fully CCW. this provides minimum pulse rate, below 1 pps. Depress PULSE ENABLE switch, wait for one green flash, and depress switch again.]

## Appendix E: Switching Transient Generator Description



**Figure E-4:** Resistor power derating for dc buses

With R selected, C provides the negative going transient envelope. In the case of Figure 2, time constant is 500  $\mu$ s. With  $R = 7 \Omega$ , the C-value would be 70  $\mu$ F. Applying a 6 dB safety margin here would result in a 1 ms duration using a 140  $\mu$ F capacitor. Note that here a safety margin can only be applied to time duration; the spike amplitude cannot be driven negative.

### E2.2 SETUP

#### WARNING!

When connecting an oscilloscope across a power bus, precautions must be made. Never connect neutral or return to a conventional scope ground unless that return or neutral is chassis grounded on the EUT side of the LISN. If the scope itself has a floating ground (this last highly recommended for this type of measurement) then that ground can be connected to any portion of the test setup. Also, regardless of whether the scope has a floating ground or not, no other connection from the scope to anywhere should be made except (when necessary, as described below) the "AC TRIGGER OUT" may be connected to the other channel.

## Appendix E: Switching Transient Generator Description

Having chosen appropriate switched RC values for the STS-1, it can now be connected into the EMI test setup. This is per Figure E-1. Also please refer to photos at end of this appendix. Actual connections from the LISN are provided on the STS-1 back panel and are so labeled (LISN HOT and LISN RTN OR GROUND). The RC values are connected across the back panel terminals so labeled. If the capacitor is polarized, be careful to connect the positive side to the red terminal. If the switched bus potential is considered a safety hazard, mount the R&C in the enclosed housing provided, again noting proper polarization (red is hot). If the bus potential is ac, provide a clean source of ac power to the back panel terminals so labeled. Clean power means that if the LISN is fed from filtered power within a shielded/screened enclosure, the ac sync source should originate outside the room, so that the entire attenuation associated with the room filtering is available to attenuate the induced spike from the sync source. Otherwise, the spike will be noisy and jittery. STS-1 ac power is also applied to the back panel.

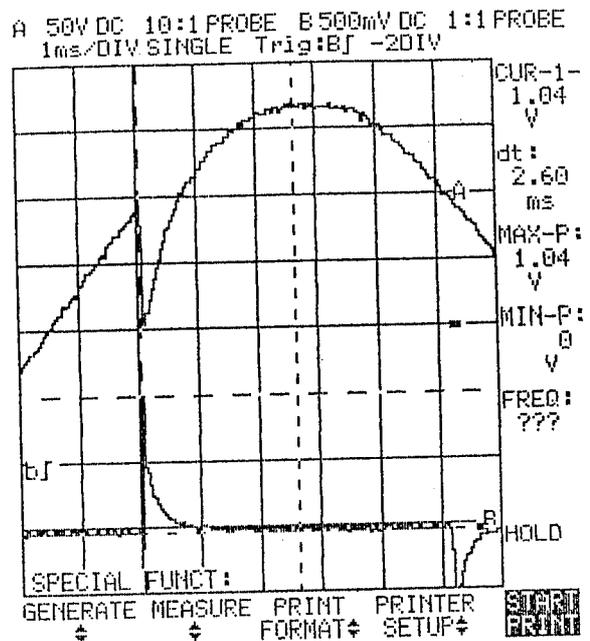
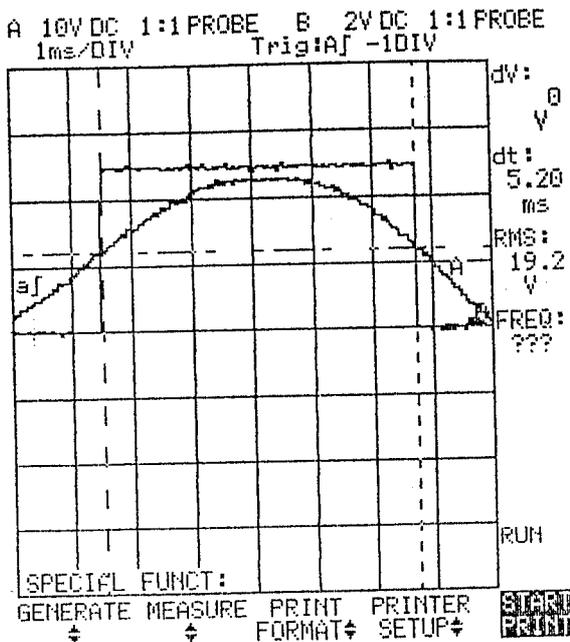
The EUT is powered from the same LISN output power port(s) and the STS-1. EUT and STS-1 both look back into the LISN as a common source impedance.

### E2.3 OPERATION

Once setup is complete, STS-1 front panel controls may be properly adjusted. Operation on a dc bus is simpler, it is described first. The knob labeled PPS adjusts the number of transients per unit time. Range is from under one pulse per second to just over 10 pps. The "BUS" switch should be set to dc. "PHASE ANGLE" only applies to ac buses. The large knob labeled "TRANSIENT MODE" selects three types of transients. "ON" selects series of the relatively long negative going transients. This simulates many loads being brought on-line sequentially. "OFF" selects a series of the short duration positive spikes. This simulates many loads being turned off sequentially. "ON/OFF" selects a series of alternately appearing negative and positive spikes. "AC POLARITY" only applies to ac buses. The "PULSE ENABLE" switch actually commands switching to occur. Actual switching rate may be monitored before switching is commanded on at the front panel BNC connector labeled PPS. It is easy to record the transient, even though it is a short duration, low duty cycle phenomenon. Use a digital oscilloscope (10 MHz single-event bandwidth - Nyquist criteria - is sufficient). Trigger on a level either above or below nominal with suitable slope as appropriate. Use a time per division near the expected transient duration. This will be on the order of 100  $\mu$ s/division for the negative going transient, but 1  $\mu$ s/division for the positive spike.

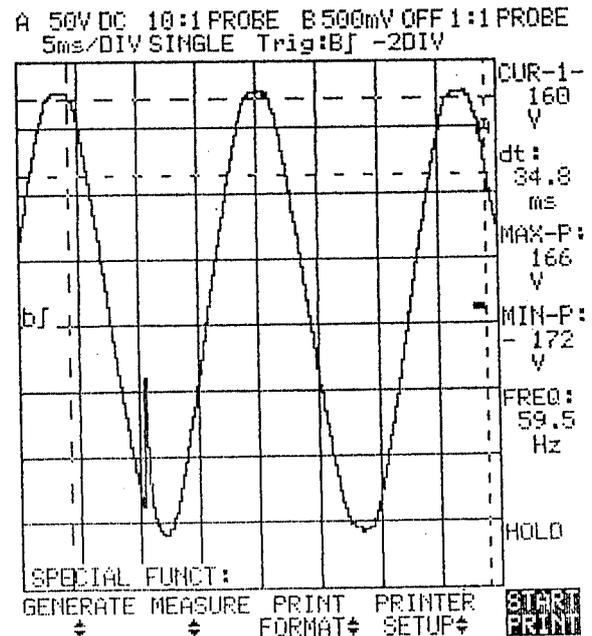
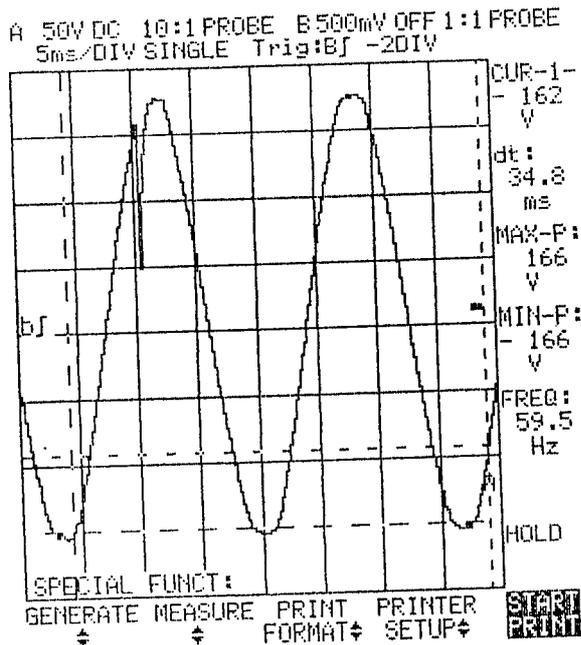
If the EUT runs off an ac bus, the following extra settings must be adjusted. The "BUS" switch must be set to either 50/60 or 400 Hz, as applicable. Phase angle (at what point along the ac waveform switching is to occur) is selected as follows. Connect "AC reference" to oscilloscope channel A. Connect "PHASE ANGLE MONITOR" to channel B. Adjust "PHASE ANGLE" knob until channel B rectangular waveform rise leading and falling edges intercept desired phase point along channel A rectified ac waveform. Oscillographs E-1 and E2 illustrate the technique. When trying to record a transient on the ac bus, a special external trigger "AC TRIGGER OUT" must be used. Connect Channel B to this port. Set the trigger to Channel B, with trigger point about 0.5 Volt. Select a positive 0.5 Volt and positive slope for recording a turn-on transient, and a negative 0.5 Volt and a negative slope when recording a turn-off transient. The AC TRIGGER OUT is isolated from chassis, so the ac bus ground scheme is not compromised.

## Appendix E: Switching Transient Generator Description



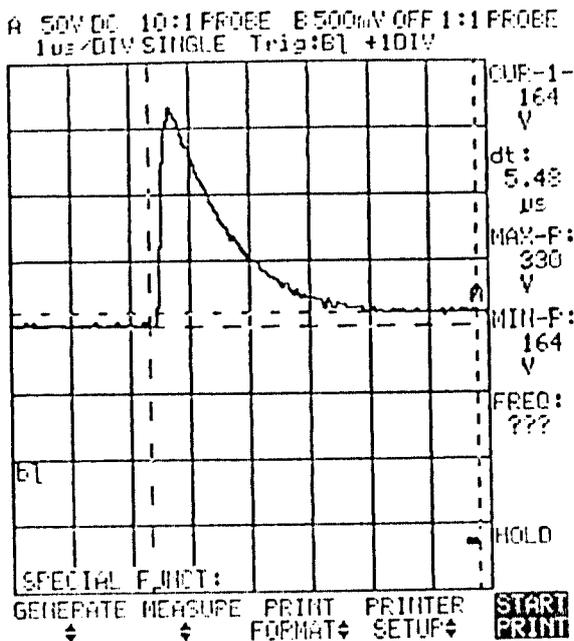
**Oscilloscope E-1:** *Ac reference and phase adjustment*      **Oscilloscope E-2:** *Actual switched ac bus and isolated trigger signal used to capture it*

The "AC POLARITY" switch selects whether the transient occurs during a positive or negative half cycle of the ac waveform. The same RC load is switched in oscilloscopes E-3 and E-4 (turn-on) and E-5 and E-6 (turn-off), but the AC POLARITY switch has been toggled.

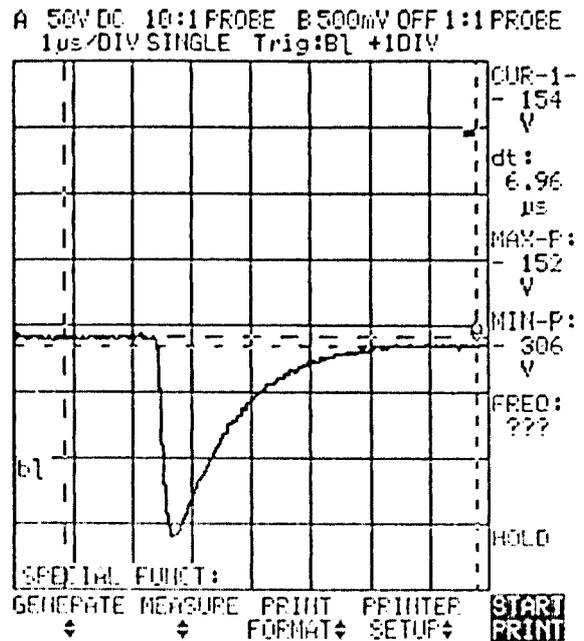


**Oscilloscope E-3:** *Turn-on transient during positive half cycle*      **Oscilloscope E-4:** *Turn-on transient during negative half cycle*

## Appendix E: Switching Transient Generator Description



**Oscilloscope E-5:** Turn-off transient during positive half cycle



**Oscilloscope E-6:** Turn-off transient during negative half cycle

### E3. STS-1 CIRCUIT DESCRIPTION

Please refer to the enclosed schematic (Figure E-3) to follow the description.

Two low voltage power supplies are utilized. These develop 5 Vdc and 12 Vdc. 5 Vdc is referenced to chassis ground. 12 Vdc is referenced to the low side of the rectified bus potential. This 12 Volts is used to drive the actual switching elements which must be referenced to the low side of the (rectified) EUT power bus. For this reason, NEVER OPERATE STS-1 WITH LID OFF. DANGEROUS POTENTIALS EXIST, NOT ONLY AT AC TRANSFORMER INPUTS AND AC SYNC, WHERE EXPECTED, BUT ALSO ALL 12 VDC CIRCUITS. For instance, if the EUT bus were 270 Vdc, the 12 Vdc reference would be at 270 Vdc, and 12 Vdc would actually be at 282 Vdc.

12 Vdc is routed to the front panel "PULSE ENABLE" switch. When that switch is off, timing may be measured from the front panel, but no power switching occurs.

The timer circuit is implemented using a 555 timer configured as an astable multivibrator. Pulse periods are selected via a front panel DPDT switch labeled according to the different kinds of buses. Pulse repetition rate is adjusted via a 1 M $\Omega$  front panel potentiometer. A 120 k $\Omega$  resistor in series with the pot bounds the selectable rate. 555 output is inverted using a switching transistor and is fed to the next stage of the circuit.

An AC sync circuit generates a 5 Vdc pulse whose leading and trailing edges line up with the desired switching point along the ac waveform. A clean source of ac power is applied to the input transformer. Transformer output is fed to a front panel DPDT switch labeled "AC POLARITY". This switch determines which phase (positive or negative) gets fed to the half-

## Appendix E: Switching Transient Generator Description

wave diode rectifier. Rectifier output gets fed (through a 10 k $\Omega$  current limiter) to the front panel BNC connector labeled "AC REFERENCE". It also is fed to a resistive divider made up in part of a front panel 5 k $\Omega$  audio taper pot labeled "PHASE ANGLE". This pot adjusts base drive into a switching transistor. To get proper polarity, a second switching transistor is configured as an inverter. The output of this second stage is fed into the next circuit via the front panel DPDT switch labeled "BUS". It is also fed to a front panel BNC connector labeled "PHASE ANGLE MONITOR" via a 10 k $\Omega$  current limiter.

The inverted 555 output is fed into a two input NAND gate, one of four in a 7400 package (pins 1&2). The other input of this NAND gate comes from the other half of the front panel "BUS" DPDT switch. The output of this switch is either the ac sync timing circuit (for ac bus selection, either 50/60 or 400 Hz) or 5 Vdc for dc bus selection. Both these inputs also tie to pins 12 and 13 of the fourth NAND gate in the 7400 package. Pin 3, the first NAND gate output ties to both pins 4&5 of the second NAND gate, configured as an inverter. But the interconnection is connected to ground by two 1  $\mu$ F tantalum capacitors. These provide a 100  $\mu$ s time delay relative to the exact same connections on the other side of the 7400 which is implemented without caps. Pin 6, the second NAND gate output is fed to a front panel BNC connector labeled "PPS" via a 10 k $\Omega$  current limiter. It is also buffered via a switching transistor and fed to an opto-isolator circuit which interfaces with 12 Volt logic. This opto-isolator eventually controls the FET which switches the RC load on and off the bus.

On the other side of the 7400 chip, the exact same symmetry is found, minus the delay caps. The output of the two NAND gates on this side are fed into the front panel DP3T switch labeled "TRANSIENT MODE SELECT". The third input on this channel of the switch is 5 Vrtn. Depending on which type of transient is selected ("ON" / "OFF" / "ON/OFF") one of these three inputs is selected to drive another opto-isolator interfacing with 12 Volt logic. This opto-isolator eventually controls a FET which can short out the LISN source impedance. When the front panel switch selects an "ON" transient, the NAND gate output is such that it commands this "shorting" FET to turn off 100  $\mu$ s in advance of the switching FET turning on. This ensures that when the RC load is switched on, the current will be drawn through the LISN. But 100  $\mu$ s before the switching LISN turns off, the shorting LISN will turn on, shorting the bus (ac-wise, through a 1.25  $\mu$ F cap) to ground. The LISN is bypassed by 1.25  $\mu$ F, and the LISN doesn't generate the positive spike. Similarly, if the "OFF" transient is selected, the NAND gate output commands the shorting FET to turn on 100  $\mu$ s prior to the switching FET turning on. The 1.25  $\mu$ F cap shorts the LISN, and the turn-on transient is vastly attenuated. 100  $\mu$ s before the switching FET turns off, the shorting FET turns off, allowing the LISN to react when the switching FET opens up.

Both opto-isolators are configured identically, except that the one controlling the switching FET drives a front panel LED which turns on for each switching event. The output of each opto-isolator goes to another PCB which contains all the power switching elements. A 510  $\Omega$  current limiting resistor is placed in series between the 7400 or switching transistor 5 Volt output and the diode input of the opto-isolators.

The opto-isolator outputs each drive IR2121 FET drivers. These circuits allow fast turn-on/off of the switching and shorting FETs. The switching FET drain is connected to the low side of the RC values connected to the back panel. The source is connected to the low side of the rectified bus potential. When the switching FET is turned on, the RC components are referenced

## Appendix E: Switching Transient Generator Description

momentarily to ground and a circuit is completed. When the FET is turned off, the circuit is broken. Note that the rectified bus potential is applied at all times to the high side of the RC components. Also note the normally open relay installed between R and C. This relay is commanded by the DP3T front panel switch labeled "TRANSIENT MODE SELECT". When either "ON" or "ON/OFF" is selected, 12 Volts is connected to the NO relay coil and it is closed, placing the capacitor in parallel with the resistor. When "OFF" is selected, the relay is not energized, and the capacitor is not energized by the rectified bus potential. This aids in snubbing the undesired turn-on transient.

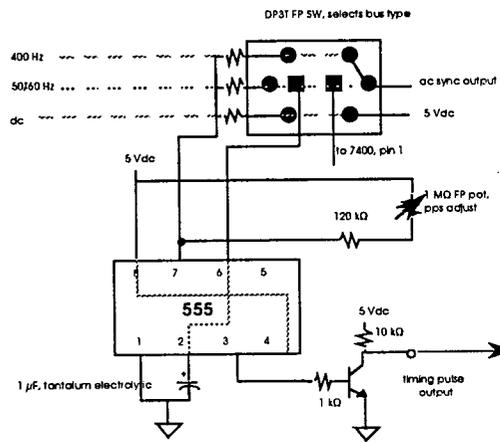
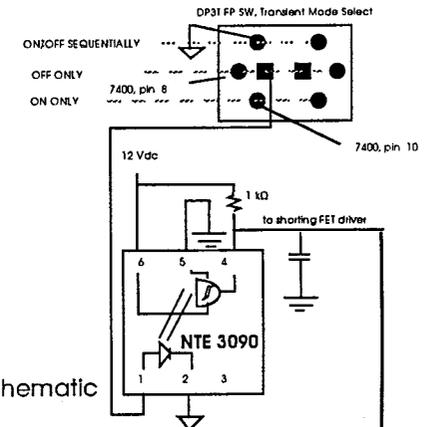
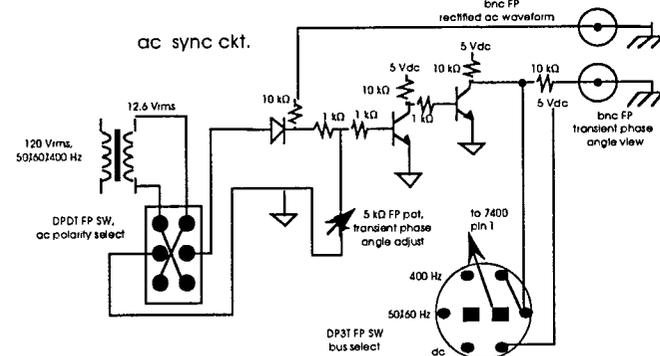
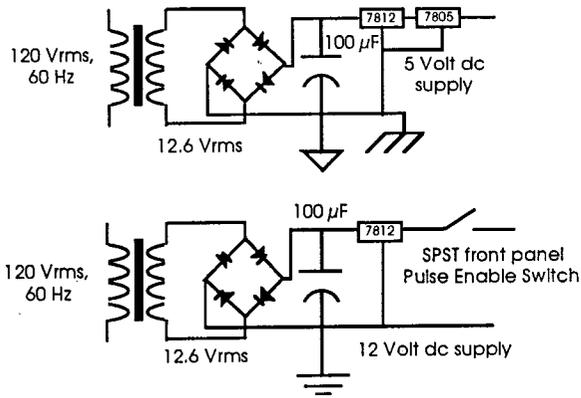
### E3.1 PARTS DESCRIPTION

All resistors are quarter Watt. All transistors are general purpose switching transistors. The PCB was laid out single-sided. This made for easy board fabrication, but messy board I/O. A two-sided approach is recommended, with I/O run out to edge connections on second side. Power supply rectifier bridges are 6 pin DIP packages with four pins. Rectifier diode for ac sync circuit is general purpose switching diode.

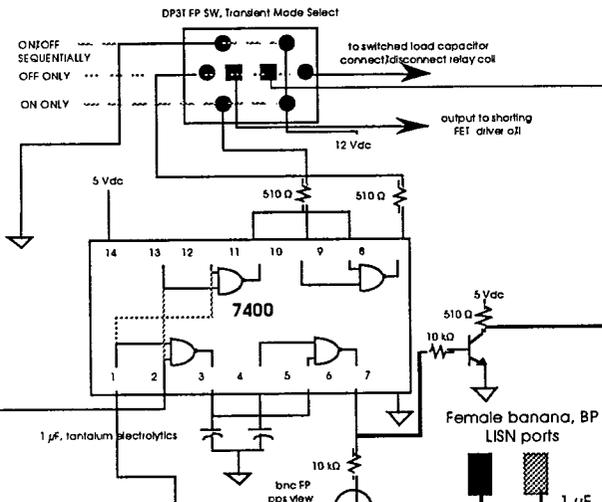
With the following exceptions, all circuit components are available at Radio Shack. The exceptions are:

- power FETs: IXYS IXFH26N50 used as switching FET, and International Rectifier IRFP450 as shorting FET.
- FET drivers: International Rectifier IR2121
- opto-isolators: NTE 3090
- switches more complex than DPDT
- Rf quality 1.25  $\mu$ F shorting cap rated at 400 Vdc
- 25 A, 600 Volt EUT power bus full-wave rectifier bridge
- Isolated bnc feedthrough connector

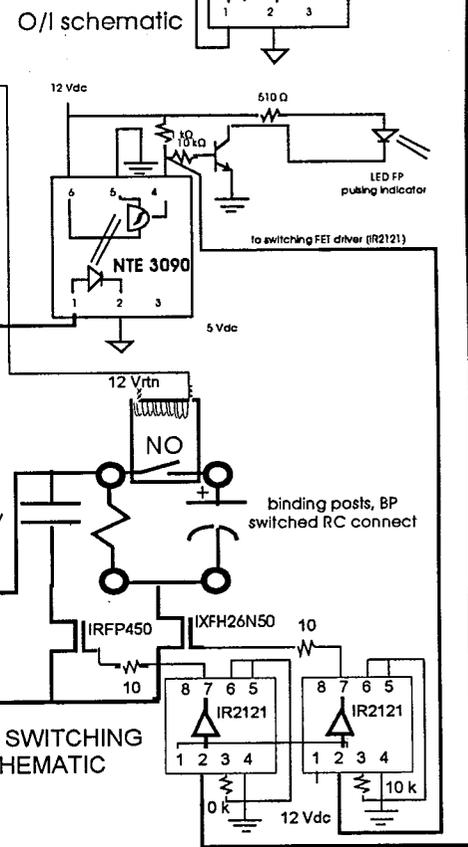
Note: Figure E-7: Switching Transient generator schematic on following page.



timer circuit with discrete pw selection



logic ckt, discrete pw select



LOAD SWITCHING SCHEMATIC

Appendix E: Switching Transient Generator Description

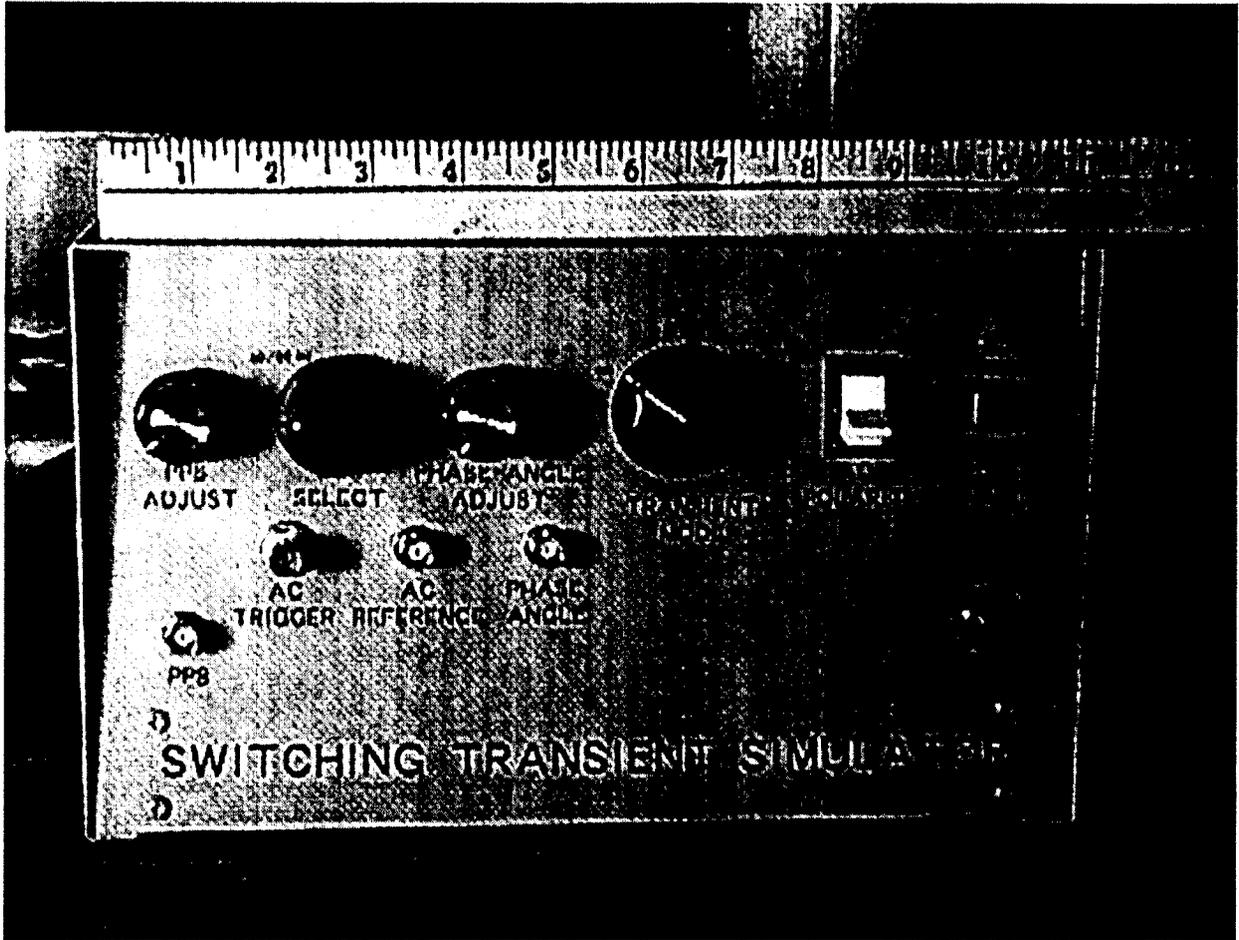


Plate E-1: *Front panel of switching transient simulator, designated STS-1*

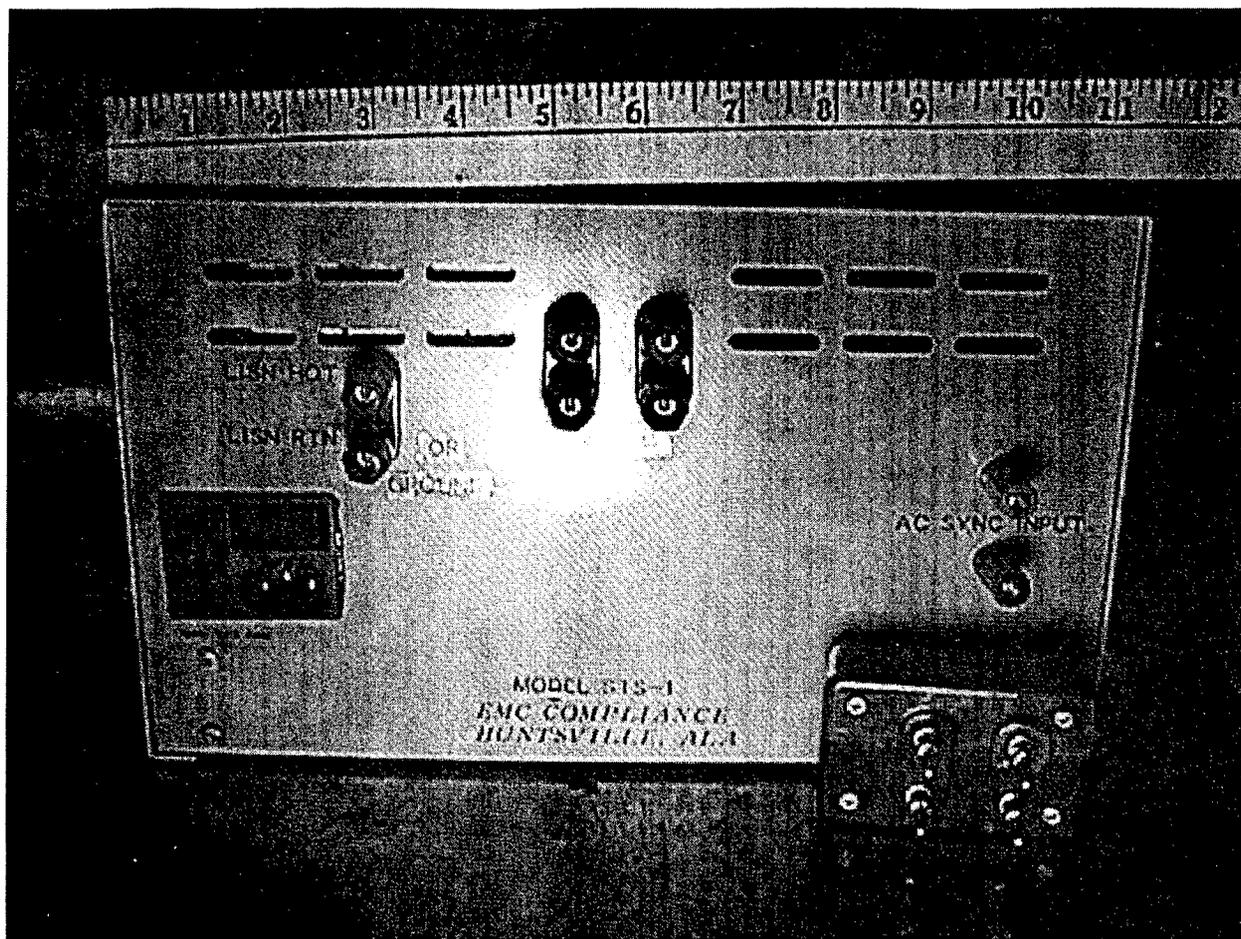


Plate E-2: Rear panel of switching transient simulator, designated STS-1

# REPORT DOCUMENTATION PAGE

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<b>13. ABSTRACT (Maximum 200 words)</b>  There have been several instances of susceptibility to switching transients. The Space Shuttle Spacelab Remote Acquisition Unit (RAU—a standard interface between Spacelab payloads and the Shuttle communications system) will shut down if the input 28 Vdc bus drops below 22 volts for more than 80 $\mu$ s. Although a MIL-STD-461 derivative CS06 requirement was levied on the RAU, it failed to find this susceptibility. A heavy payload on one aircraft sags the 28 volt bus below 20 volts for milliseconds. Dc-dc converters have an operating voltage. A typical 28 Vdc-to-5 Vdc converter operates within tolerance when input potential is between 17-40 Vdc. A hold-up capacitor can be used to extend the time this range is presented to the converter when the line potential sags or surges outside this range. The designer must know the range of normal transients in order to choose the correct value of hold-up.  This report describes the phenomena of electrical power bus transients induced by the switching of loads both on and off the bus, and control thereof.				
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